

Chapter Outline

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6.1 Introduction

We saw in Chapter 5 that transistors can be used to provide amplification of signals. The operational amplifier (or op-amp) is a high-gain, direct-coupled amplifier consisting of multiple stages: an input stage to provide a high input resistance with a certain amount of voltage gain, a middle stage to provide a high voltage gain, and an output stage to provide a low output resistance. It operates with a differential voltage between two input terminals, and it is a complete, integrated-circuit, prepackaged amplifier. An op-amp, often referred to as a linear (or analog) integrated circuit (IC), is a very popular and versatile integrated circuit. It serves as a building block for many electronic circuits. For most applications, knowledge of the terminal characteristics of op-amps is all you need to design op-amp circuits. However, for some applications requiring precision, internal knowledge of op-amps is necessary.

The learning objectives of this chapter are as follows:

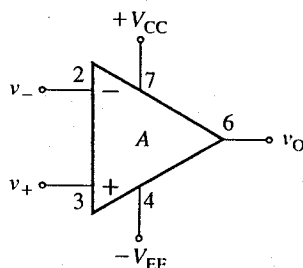
- To learn about the external characteristics of op-amps and how to model op-amps
- To analyze and design op-amp circuits
- To learn about the usefulness of op-amps in signal conditioning

6.2

Characteristics of Ideal Op-Amps

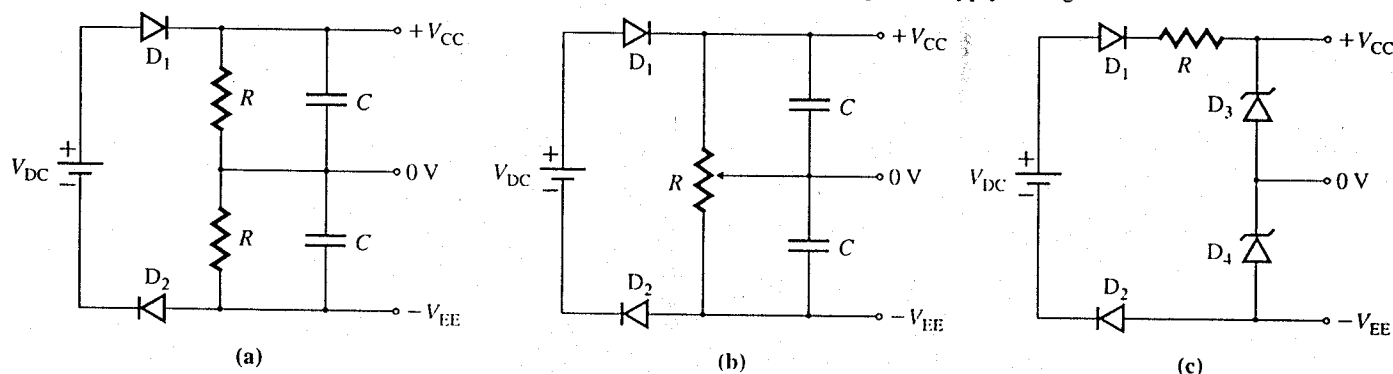
FIGURE 6.1

Symbol for an op-amp



The symbol for an op-amp is shown in Fig. 6.1. An op-amp has at least five terminals. Terminal 2 is called the “inverting input” because the output that results from input at this terminal will be inverted. Terminal 3 is called the “noninverting input” because the output that results from input at this terminal will have the same polarity as the input. Terminal 4 is for negative dc supply V_{EE} . Terminal 6 is the output terminal. Terminal 7 is for positive dc supply V_{CC} .

Instead of using two dc power supplies, one can generate V_{CC} and V_{EE} from a single power supply V_{DC} , as shown in Fig. 6.2(a). The value of R should be high enough (usually, $R \geq 10 \text{ k}\Omega$) that it does not draw much current from the dc supply V_{DC} . Capacitors are used for decoupling (bypass) of the dc power supply, and the value of C is typically in the range of $0.01 \mu\text{F}$ to $10 \mu\text{F}$. Instead of two resistors, a potentiometer can be used to ensure that $V_{CC} = V_{EE}$, as shown in Fig. 6.2(b). Diodes D_1 and D_2 prevent any reverse current flow; they are often used to protect the op-amp in case the positive and negative terminals of the supply voltages V_{DC} are reversed accidentally. Also, two zener diodes can be used to obtain symmetrical supply voltages, as shown in Fig. 6.2(c). The value of R should be low enough to force the zener diodes to operate in the zener or avalanche mode. It should be noted that this circuit will not work if the dc supply comes with a ground.

FIGURE 6.2 Arrangements for positive and negative supply voltages

The output voltage of an op-amp is directly proportional to the small-signal differential (or difference) input voltage. Thus, an op-amp can be modeled as a voltage-controlled voltage source; its equivalent circuit is shown in Fig. 6.3(a). The output voltage v_O is given by

$$v_O = -A_o v_d = -A_o (v_+ - v_-) \quad (6.1)$$

where

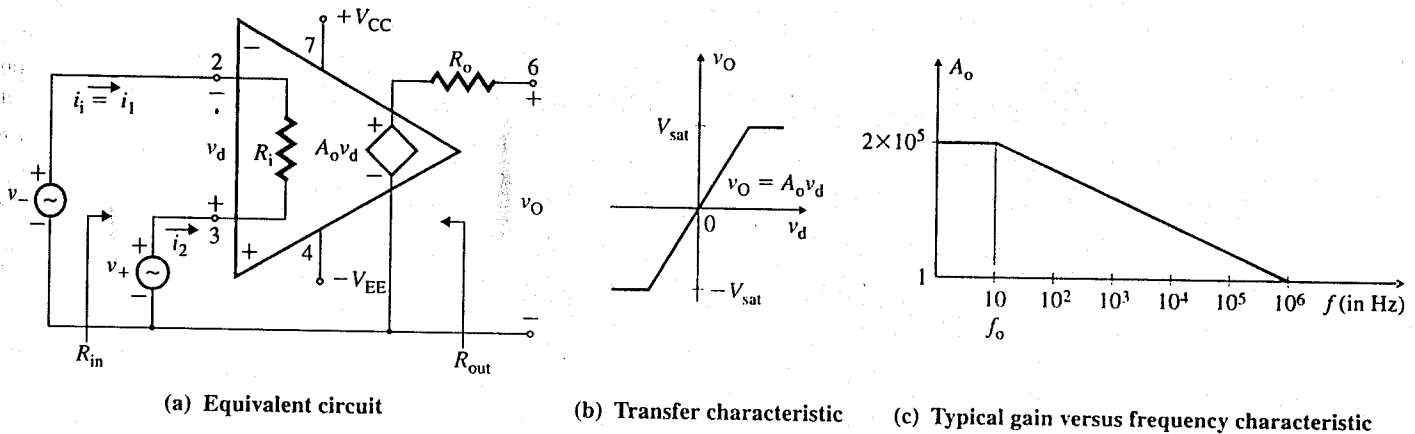
A_o = small-signal open-loop voltage gain

v_d = small-signal differential (or difference) input voltage

v_- = small-signal voltage at the inverting terminal with respect to the ground

v_+ = small-signal voltage at the noninverting terminal with respect to the ground

Input resistance R_i is the equivalent resistance between the differential input terminals. The input resistance of an op-amp with a BJT input stage is very high, with a typical value of $2 \text{ M}\Omega$. Op-amps with an FET input stage have much higher input resistances (i.e., $10^{12} \Omega$). Therefore, the input current drawn by the amplifier is very small (typically on the order of nA), tending to zero.

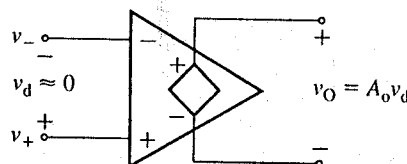
FIGURE 6.3 Equivalent circuit of an op-amp

Output resistance R_o is Thevenin's equivalent resistance. It is usually in the range of 10 to 100 Ω , with a typical value of 75 Ω . Its effective value is reduced, however, when external connections are made; then R_o can be neglected for most applications.

Open-loop differential voltage gain A_o is the differential voltage gain of the amplifier with no external components. It ranges from 10^4 to 10^6 , with a typical value of 2×10^5 . Since the value of A_o is very large, v_d becomes very small (typically on the order of μV), tending to zero. The transfer characteristic (v_o versus v_d) is shown in Fig. 6.3(b). In reality, the output voltage cannot exceed the positive or negative saturation voltage $\pm V_{sat}$ of the op-amp, which is set by supply voltages V_{CC} and V_{EE} , respectively. The saturation voltage is usually 1 V lower than the supply voltage V_{CC} or V_{EE} . Thus, the output voltage will be directly proportional to the differential input voltage v_d only until it reaches the saturation voltage; thereafter the output voltage remains constant. The gain of practical op-amps is also frequency dependent. A typical gain-versus-frequency characteristic is shown in Fig. 6.3(c). The typical value of the cut-off frequency f_o is 10 Hz, with a typical gain bandwidth of 1 MHz. Note that the model in Fig. 6.3(a) does not take into account the saturation effect and assumes that gain A_o remains constant for all frequencies.

The analysis and design of circuits employing op-amps can be greatly simplified if the op-amps in the circuit are assumed to be ideal. Such an assumption allows you to approximate the behavior of the op-amp circuit and to obtain the approximate values of circuit components that will satisfy some design specifications. Although the characteristics of practical op-amps differ from the ideal characteristics, the errors introduced by deviations from the ideal conditions are acceptable in most applications. A complex op-amp model is used in applications requiring precise results. The circuit model of an ideal op-amp is shown in Fig. 6.4; its characteristics are as follows:

- The open-loop voltage gain is infinite: $A_o = \infty$.
- The input resistance is infinite: $R_i = \infty$.
- The amplifier draws no current: $i_i = 0$.
- The output resistance is negligible: $R_o = 0 \Omega$.
- The gain A_o remains constant and is not a function of frequency.

FIGURE 6.4
Model of an ideal op-amp

- The output voltage does not change with changes in power supplies. This condition is generally specified in terms of the *power supply sensitivity* PSS: $PSS = 0$.
- An op-amp is a differential amplifier, and it should amplify the differential signal appearing between the two input terminals. Any signal that is common to two inputs (i.e., noise) should not be amplified and should not appear in the output. Thus, the differential gain (due to a differential signal) should tend to infinity, and the common mode gain (due to a common signal) should tend to zero. The condition is generally specified in terms of the *common mode rejection ratio* CMRR: $CMRR = \infty$. This ratio is discussed in Sec. 7.3.

EXAMPLE 6.1

Finding the differential input voltage and input current of an op-amp The op-amp of Fig. 6.3(a) has an open-loop gain of $A_o = 2 \times 10^5$. The input resistance is $R_i = 0.6 \text{ M}\Omega$. The dc supply voltages are $V_{CC} = 12 \text{ V}$ and $-V_{EE} = -12 \text{ V}$.

- What value of v_d will saturate the amplifier?
- What are the values of the corresponding input current i_i ?

SOLUTION

- $v_d = v_O / A_o = \pm 12 / (2 \times 10^5) = \pm 60 \text{ }\mu\text{V}$
- $i_i = -v_d / R_i = \pm 60 \text{ }\mu\text{V} / 0.6 \text{ M}\Omega = \pm 0.1 \text{ nA}$

EXAMPLE 6.2

Finding the maximum output voltage of an op-amp The op-amp of Fig. 6.3(a) has $A_o = 2 \times 10^5$, $R_i = 2 \text{ M}\Omega$, $R_o = 75 \text{ }\Omega$, $V_{CC} = 12 \text{ V}$, and $-V_{EE} = -12 \text{ V}$. The maximum possible output voltage swing is $\pm 11 \text{ V}$. If $v_- = 100 \text{ }\mu\text{V}$ and $v_+ = 25 \text{ }\mu\text{V}$, determine the output voltage v_O .

SOLUTION

From Eq. (6.1),

$$v_O = A_o(v_+ - v_-) = 2 \times 10^5 \times (25 - 100) \times 10^{-6} = -15 \text{ V}$$

Because of the saturation, the output voltage cannot exceed the maximum voltage limit of -11 V , and therefore $v_O = -11 \text{ V}$.

KEY POINTS OF SECTION 6.2

- An op-amp is a direct-coupled differential amplifier. It has a high gain (typically 2×10^5), a high input resistance (typically $1 \text{ M}\Omega$), and a low output resistance (typically $50 \text{ }\Omega$).
- An ideal op-amp has the characteristic of infinite gain, infinite input resistance, and zero output resistance.
- An op-amp requires dc power supplies, and the maximum output voltage swing is limited to the dc supply voltages.

6.3

Op-Amp
PSpice/SPICE
Models

There are many types of op-amps, as we will see in Chapter 15. An op-amp can be simulated from its internal circuit arrangement. The internal structure of op-amps is very complex, however, and differs from one model to another. For example, the $\mu\text{A}741$ type of general-purpose op-amp consists of 24 transistors. It is too complex for the student version of the PSpice circuit simulation software to analyze; however, a macromodel, which is a simplified version of the op-amp and requires only two transistors, is quite accurate for many applications and can be simulated as a subcircuit or a library file [6]. Some

manufacturers of op-amps supply macromodels of their products [5]. The student version of PSpice has a library called NOM.LIB, which contains models of three common types of op-amps: μ A741, LM324, and LF411. The parameters of the three op-amps for the circuit model in Fig. 6.3(a) are as follows:

- The μ A741 op-amp is a general-purpose op-amp with a BJT input stage. It is capable of producing output voltages of ± 14 V with dc power supply voltages of ± 15 V. The parameters are $R_i = 2 \text{ M}\Omega$, $R_o = 75 \Omega$, $A_o = 2 \times 10^5$, break frequency $f_b = 10 \text{ Hz}$, and unity-gain bandwidth $f_{bw} = 1 \text{ MHz}$.
- The LF411 op-amp is a general-purpose op-amp with an FET input stage. It is capable of producing output voltages of ± 13.5 V with dc power supply voltages of ± 15 V. The parameters are $R_i = 10^{12} \Omega$, $R_o = 50 \Omega$, $A_o = 2 \times 10^5$, break frequency $f_b = 20 \text{ Hz}$, and unity-gain bandwidth $f_{bw} = 4 \text{ MHz}$.
- The LM324 op-amp has a BJT input stage and is used with a single dc power supply voltage. It can produce output voltages in the range from approximately 20 mV to 13.5 V with a dc supply voltage of +15 V. The parameters are $R_i = 2 \text{ M}\Omega$, $R_o = 50 \Omega$, $A_o = 2 \times 10^5$, break frequency $f_b = 4 \text{ kHz}$, and unity-gain bandwidth $f_{bw} = 1 \text{ MHz}$.

The professional version of PSpice supports library files for many devices. It is advisable to check the name of the current library file by listing the files of the PSpice programs (using DOS command DIR).

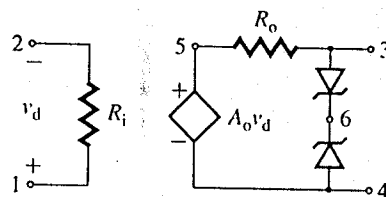
If the PSpice/SPICE model of an op-amp is not available, it is possible to represent the op-amp by simple models that give reasonable results, especially for determining the approximate design values of op-amp circuits. PSpice/SPICE models can be classified into three types: dc linear models, ac linear models, and nonlinear macromodels. Taking the μ A741 op-amp as an example, we will develop simple PSpice/SPICE models of these three types.

dc Linear Model

An op-amp may be modeled as a voltage-controlled voltage source, as shown in Fig. 6.5. Two zener diodes are connected back to back in order to limit the output swing to the saturation voltages (say, between -14 V and $+14$ V). This simple model, which assumes that the voltage gain is independent of the frequency, is suitable only for dc or low-frequency applications. The list of the PSpice/SPICE subcircuit UA741_DC for Fig. 6.5 is shown below.

```
* Subcircuit definition for UA741_DC
.SUBCKT UA741_DC 1 2 3 4
* Subcircuit name Vi+ Vi- Vo+ Vo-
RI 1 2 2MEG ; Input resistance
RO 5 3 75 ; Output resistance
EA 5 4 1 2 2E+5 ; Voltage-controlled voltage source
D1 3 6 DMOD ; Zener diode with model DMOD
D2 4 6 DMOD ; Zener diode with model DMOD
.MODEL DMOD D (BV=14V) ; Ideal zener model with a zener voltage of 14 V
.ENDS UA741_DC ; End of subcircuit definition
```

FIGURE 6.5
dc linear model



In PSpice/SPICE, the name of a subcircuit must begin with X. For example, the calling statement for the amplifier A1, which uses the subcircuit UA741_DC, is as follows:

```
XA1 5 6 7 8 UA741_DC
* Vi+ Vi- Vo+ Vo- Subcircuit name
```

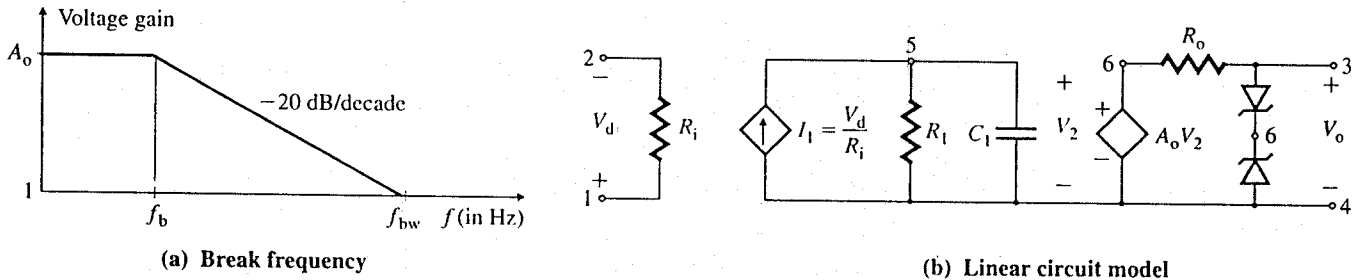
This subcircuit definition UA741_DC can be inserted into the circuit file. Alternatively, it can reside in a user-defined file, say USER.LIB in C drive, in which case the circuit file must contain the following statement:

C:USER.LIB; Library file name must include the drive and directory location

ac Linear Model

The frequency response of internally frequency-compensated op-amps can be approximated by a single break frequency, as shown in Fig. 6.6(a). This characteristic can be modeled by the circuit of Fig. 6.6(b), which is a frequency-dependent model of an op-amp. The dependent sources have a common node 4. Without this common node, PSpice/SPICE will give an error message, because there will be no dc path from the nodes of the dependent current source to the ground. The common node could be either with the input stage or with the output stage. The time constant $\tau = R_1 C_1$ gives the break frequency f_b . If an op-amp has more than one break frequency, it can be represented by using as many capacitors as there are breaks. R_i and R_o are the input and output resistances, respectively. A_o is the open-circuit dc voltage gain. Two zener diodes are connected back to back in order to limit the output swing to the saturation voltages (say, between -14 V and $+14$ V).

FIGURE 6.6 ac linear model with a single break frequency



The output voltage can be expressed in Laplace's domain as

$$V_o = A_o V_2 = \frac{A_o R_1 I_1}{1 + R_1 C_1 s} = \frac{A_o V_d}{1 + R_1 C_1 s} \quad (6.2)$$

Substituting $s = j\omega = j2\pi f$ into Eq. (6.2) gives

$$V_o = \frac{A_o V_d}{1 + j2\pi f R_1 C_1} = \frac{A_o V_d}{1 + jf/f_b} \quad (6.3)$$

which gives the frequency-dependent open-loop voltage gain of an op-amp with a single break frequency as

$$A_o(j\omega) = \frac{V_o}{V_d} = \frac{A_o}{1 + jf/f_b} \quad (6.4)$$

where $f_b = 1/(2\pi R_1 C_1)$ = break frequency, in Hz

A_o = large-signal (or dc) voltage gain of the op-amp

For $\mu A741$ op-amps, $f_b = 10$ Hz, $A_o = 2 \times 10^5$, $R_i = 2$ M Ω , and $R_o = 75$ Ω . If we let $R_1 = 10$ k Ω (used as a typical value), $C_1 = 1/(2\pi \times 10 \times 10 \times 10^3) = 1.15619$ μ F.

Note that we could also choose a different value of R_1 . The list of the PSpice/SPICE sub-circuit UA741_AC for Fig. 6.6(b) is shown below.

```
* Subcircuit definition for UA741_AC
.SUBCKT UA741_AC 1 2 3 4
* Subcircuit name Vi+ Vi- Vo+ Vo-
RI 1 2 2MEG ; Input resistance
RO 6 3 75 ; Output resistance
GB 4 5 1 2 0.1M ; Voltage-controlled current source
R1 5 4 10K
C1 5 4 1.5619UF
EA 6 4 5 4 2E+5 ; Voltage-controlled voltage source
D1 3 7 DMOD ; Zener diode with model DMOD
D2 4 7 DMOD ; Zener diode with model DMOD
.MODEL DMOD D (BV=14V) ; Ideal zener model with a zener voltage of 14 V
.ENDS UA741_AC ; End of subcircuit definition
```

Nonlinear Macromodel

The subcircuit definitions of op-amp macromodels are described by a set of .MODEL statements. The macromodels are normally simulated at room temperature and contain nominal values. The effects of temperature are not included. The library file NOM.LIB contains the subcircuit definition UA741, which can be called up by including the following general statements in the circuit file:

[illegible]

KEY POINTS OF SECTION 6.3

- An op-amp can be represented in PSpice/SPICE by one of three models: (a) a dc linear model, which is simple but suitable only for low frequencies (typically less than 20 Hz); (b) an ac linear model, which is simple and frequency dependent; (c) a nonlinear macromodel, which is more complex.
- The student version of PSpice limits the number of active devices and nodes, allowing only one macromodel in a circuit. Thus, the choice of a model depends on the complexity of the circuit; the preferred model is the macromodel, followed by the ac model and then the dc model.

6.4

Analysis of Ideal Op-Amp Circuits

In Eq. (6.1) there are three possible conditions for the output voltage v_o : if $v_- = 0$, v_o will be positive ($v_o = A_o v_+$), (b) if $v_+ = 0$, v_o will be negative ($v_o = -A_o v_-$), or (c) if both v_+ and v_- are present, $v_o = A_o(v_+ - v_-)$. Therefore, depending on the conditions of the input voltages, op-amp circuits can be classified into three basic configurations: noninverting amplifiers, inverting amplifiers, or differential (or difference) amplifiers.

Noninverting Amplifiers

The configuration of a noninverting amplifier is shown in Fig. 6.7(a). The input voltage v_S is connected to the noninverting terminal. The voltage v_x , which is proportional to the output voltage, is connected via R_1 and R_F to the inverting terminal. Using Kirchhoff's voltage law (KVL), we get

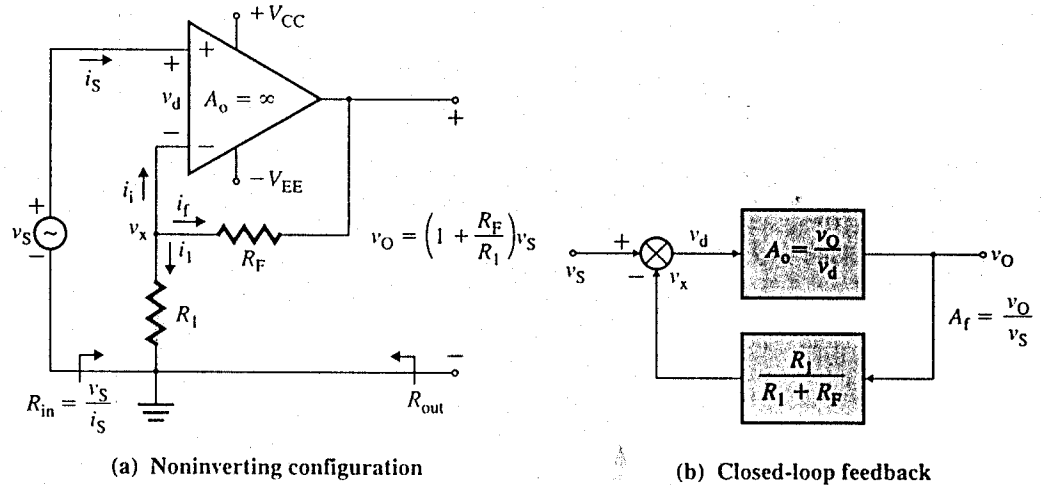
$$v_S = v_x + v_d$$

The differential voltage v_d , given by

$$v_d = v_S - v_x$$

is then amplified by the op-amp, whose output is then fed back to the inverting terminal. Thus, this is a feedback circuit; the block diagram is shown in Fig. 6.7(b). We will cover feedback in Chapter 10.

FIGURE 6.7
Noninverting amplifier



Let us assume an ideal op-amp. That is, $v_d = 0$, $i_S = 0$, and $A_o \approx \infty$. The voltage v_x at the inverting terminal is

$$v_x = v_S - v_d \approx v_S$$

Using Kirchhoff's current law (KCL) at the inverting terminal, we get

$$i_1 + i_f + i_i = 0$$

Since the current i_i drawn by an ideal op-amp is zero, $i_1 = -i_f$. That is,

$$\frac{v_x}{R_1} = -\frac{v_x - v_O}{R_F} \quad \text{or} \quad \frac{v_S}{R_1} = -\frac{v_S - v_O}{R_F}$$

which, after simplification, yields

$$v_O = \left(1 + \frac{R_F}{R_1}\right)v_S$$

giving the closed-loop voltage gain A_f as

$$A_f = \frac{v_O}{v_S} = 1 + \frac{R_F}{R_1} \quad (6.5)$$

Since the current drawn by the amplifier is zero, the effective input resistance of the amplifier is very high, tending to infinity:

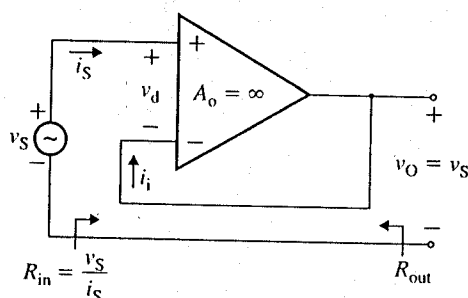
$$R_{in} = \frac{v_S}{i_S} = \infty$$

The effective output resistance is given by $R_{\text{out}} = R_o \approx 0 \Omega$. If $R_F = 0 \Omega$ or $R_1 = \infty$, as shown in Fig. 6.8, Eq. (6.5) becomes

$$A_f = 1 \quad (6.6)$$

That is, the output voltage equals the input voltage: $v_O = v_S$. The circuit of Fig. 6.8 is commonly referred to as a *voltage follower*, since its output voltage follows the input voltage. It has the inherent characteristics of a high input impedance (or resistance, typically $10^{10} \Omega$) and a low output impedance (or resistance, typically $50 \text{ m}\Omega$). The exact values can be found by applying the feedback analysis techniques discussed in Chapter 10. A voltage follower is commonly used as the *buffer stage* between a low impedance load and a source requiring a high impedance load.

FIGURE 6.8
Voltage follower



► **NOTES:**

1. The current i_S flowing into an op-amp and the differential voltage v_d are very small, tending to zero. Thus, the inverting terminal is at a ground potential with respect to the noninverting terminal, and it is said to be at the *virtual short*.
2. A_o is the open-loop voltage gain of the op-amp, whereas A_f is the closed-loop voltage gain of the op-amp circuit (or amplifier) and is dependent only on external components.
3. A noninverting amplifier can be designed to give a specified gain A_f simply by choosing the appropriate ratio R_F/R_1 . A small value of R_1 will load the amplifier and cause it to draw appreciable current, and a large value of R_F will increase the noise generated in the resistor. As a guide, all resistances in op-amp circuits should be between $1 \text{ k}\Omega$ and $10 \text{ M}\Omega$.
4. Designing a noninverting voltage amplifier is very simple: Given gain A_f , choose R_1 and then find R_F .

EXAMPLE 6.3

D

Designing a noninverting op-amp circuit Design a noninverting amplifier as shown in Fig. 6.7(a) to provide a closed-loop voltage gain of $A_f = 80$. The input voltage is $v_S = 200 \text{ mV}$ with a source resistance of $R_S = 500 \Omega$. Find the value of output voltage v_O . The dc supply voltages are $V_{CC} = -V_{EE} = 12 \text{ V}$.

SOLUTION

Choose a suitable value of R_1 : Let $R_1 = 5 \text{ k}\Omega$. Find the value of R_F from Eq. (6.5). Since $A_f = 80 = 1 + R_F/R_1$,

$$R_F/R_1 = 79$$

$$\text{and} \quad R_F = 79 \times 5 = 395 \text{ k}\Omega$$

Find the output voltage v_O from Eq. (6.5):

$$v_O = A_f v_S = 80 \times 200 \times 10^{-3} = 16 \text{ V}$$

which exceeds the maximum dc supply voltage $V_{CC} = 12 \text{ V}$. Thus, the output voltage will be $v_O = V_{CC} = 12 \text{ V}$.

- **NOTE:** R_S is in series with the op-amp input resistance R_i , which is very large in comparison to R_S . Therefore, R_S will not affect the closed-loop gain A_f .

EXAMPLE 6.4

Finding the voltage gain of a noninverting op-amp circuit For the noninverting amplifier in Fig. 6.7(a), the input voltage is $v_S = 100$ mV with a source resistance of $R_S = 500 \Omega$. The circuit parameters are $R_F = 395$ k Ω , $R_1 = 5$ k Ω , and $A_o = 2 \times 10^5$. Calculate (a) the closed-loop gain A_f , (b) the output voltage v_O , and (c) the errors in the output voltage v_O and the gain A_f if A_o tends to infinity.

SOLUTION

Since the current drawn by the op-amp is zero, $i_1 = -i_F$. That is,

$$\frac{v_x}{R_1} = -\frac{v_x - v_O}{R_F}$$

which gives

$$v_x = \frac{R_1}{R_1 + R_F} v_O \quad (6.7)$$

The output voltage v_O is

$$v_O = A_o(v_S - v_x) = A_o v_d \quad (6.8)$$

The input voltage at the noninverting terminal is the sum of v_x and v_d . That is,

$$v_S = v_x + v_d$$

which, after substitution of v_x from Eq. (6.7) and v_d from Eq. (6.8), becomes

$$v_S = \frac{R_1 v_O}{R_1 + R_F} + \frac{v_O}{A_o} = v_O \left(\frac{R_1}{R_1 + R_F} + \frac{1}{A_o} \right)$$

Thus, the closed-loop voltage gain A_f is given by

$$A_f = \frac{v_O}{v_S} = \frac{A_o(R_1 + R_F)}{A_o R_1 + R_1 + R_F} = \frac{1 + R_F/R_1}{1 + (1 + R_F/R_1)/A_o} = \frac{1 + R_F/R_1}{1 + x} \quad (6.9)$$

$$\text{where } x = \frac{1}{A_o} \left(1 + \frac{R_F}{R_1} \right) \quad (6.10)$$

For a small value of x , which is usually the case, $(1 + x)^{-1} \approx 1 - x$, and Eq. (6.9) can be approximated by

$$A_f = \left(1 + \frac{R_F}{R_1} \right) (1 - x) \quad (6.11)$$

Therefore, the error introduced for a finite value of gain A_o is x .

(a) From Eq. (6.10),

$$x = (1 + 395/5)/(2 \times 10^5) = 40 \times 10^{-5} = 40 \times 10^{-3}\%$$

From Eq. (6.9),

$$A_f = (1 + 395/5)/(1 + 40 \times 10^{-5}) = 79.968$$

(b) The output voltage v_O is

$$v_O = A_s v_S = 79.9992 \times 100 \times 10^{-3} = 7.9968 \text{ V}$$

(c) From Eq. (6.11), the error in the output voltage v_O is

$$\Delta v_O = -x(1 + R_F/R_1) = -40 \times 10^{-5} \times 80 = -32 \text{ mV, or } 0.04\%$$

The error in the gain A_f is

$$\Delta A_f = -x = -40 \times 10^{-5} = -0.04\%$$

- **NOTE:** In order to minimize the dependency of the closed-loop gain A_f on the open-loop gain A_o , the value of x should be made very small. That is,

$$A_o \gg \left(1 + \frac{R_F}{R_1}\right) \quad (6.12)$$

This condition is often satisfied by making A_o at least ten times larger than $(1 + R_F/R_1)$. That is,

$$\left(1 + \frac{R_F}{R_1}\right) \leq 0.1A_o \quad (6.13)$$

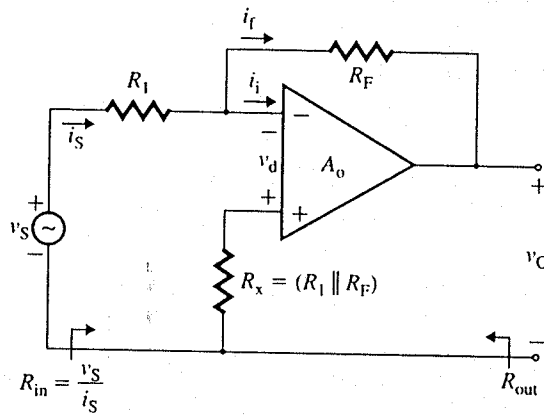
Inverting Amplifiers

Another common configuration is the inverting voltage amplifier, as shown in Fig. 6.9. R_F is used to feed the output voltage back to the inverting terminal of the op-amp. Using Kirchhoff's voltage law, we have

$$v_S = R_1 i_S - v_d \quad (6.14)$$

$$-v_d = R_F i_f + v_O \quad (6.15)$$

FIGURE 6.9
Inverting amplifier



Using Kirchhoff's current law at the inverting terminal, we get

$$i_S = i_f + i_i \quad (6.16)$$

For an ideal op-amp, $v_d \approx 0$ and $i_i \approx 0$. That is, Eq. (6.14) becomes

$$v_S = R_1 i_S$$

which gives

$$i_S = \frac{v_S}{R_1}$$

Also, $R_F i_f + v_O = 0$, which gives the feedback current as

$$i_f = -\frac{v_O}{R_F}$$

For $i_i \approx 0$, Eq. (6.16) becomes

$$i_S = i_f \quad \text{or} \quad \frac{v_S}{R_1} = -\frac{v_O}{R_F}$$

Therefore, the output voltage is related to the input voltage by

$$v_O = -\left(\frac{R_F}{R_1}\right)v_S \quad (6.17)$$

which gives the closed-loop voltage gain of the op-amp circuit as

$$A_f = \frac{v_O}{v_S} = -\frac{R_F}{R_1} \quad (6.18)$$

Since $v_d \approx 0$, the effective input resistance R_{in} of the amplifier is given by

$$R_{in} = \frac{v_S}{i_S} = \frac{v_S}{(v_S + v_d)/R_1} \approx R_1$$

The effective output resistance is given by $R_{out} = R_o \approx 0 \Omega$.

► **NOTES:**

1. The negative sign in Eq. (6.17) signifies that the output voltage is out of phase with respect to the input voltage by 180° (in the case of an ac input) or of opposite polarity (in the case of a dc input).
2. The current i_i flowing into the op-amp is very small, tending to zero, and the voltage v_d at the inverting terminal is also very small, tending to zero. Although the inverting terminal is not the ground point, this terminal is said to be a virtual short.
3. An inverting amplifier can be designed to give a specified gain simply by choosing the appropriate ratio R_F/R_1 . A small value of R_1 will load the input source, and a large value of R_F will increase the noise generated in the resistor. As a guide, all resistances in op-amp circuits should be between 1 k Ω and 10 M Ω .
4. If $R_1 = R_F$, Eq. (6.18) gives $A_f = -1$ and $v_O = -v_S$. The circuit then behaves as a *unity-gain inverter* (or simply an *inverter*).
5. Designing an inverting voltage amplifier is straightforward: Given R_{in} and gain A_f , find R_1 and then find R_F .

EXAMPLE 6.5

D

Designing an inverting op-amp circuit to limit the input current A transducer produces a voltage signal of $v_S = 100$ mV with an internal resistance of $R_s = 2$ k Ω . Design the inverting op-amp amplifier of Fig. 6.9 by determining the values of R_1 , R_F , and R_x . The output voltage should be $v_O = -8$ V. The current drawn from the transducer should not be more than 10 μ A. Assume an ideal op-amp and $V_{CC} = V_{EE} = 15$ V.

SOLUTION

$R_s = 2$ k Ω , $v_S = 100$ mV, and $v_O = -8$ V. The source resistance R_s (not shown in Fig. 6.9) is in series with R_1 . Let

$$R'_1 = R_1 + R_s$$

The maximum input current is

$$i_{S(max)} = 10 \mu\text{A}$$

The minimum input resistance is

$$R_{in(min)} = v_S / i_{S(max)} = 100 \text{ mV} / 10 \mu\text{A} = 10 \text{ k}\Omega$$

Thus, $R_F = 8(R_1 + R_s) = 8R'_1 = 80 \times 10 \text{ k}\Omega = 800 \text{ k}\Omega$

and $A_f = v_O / v_S = -8 / (100 \times 10^{-3}) = -80$

From Eq. (6.18),

$$-80 = -R_F / R'_1 = -R_F / (R_1 + R_s)$$

Thus, $R'_1 = R_1 + R_s = R_{in(min)} = 10 \text{ k}\Omega$

or $R_1 = R'_1 - R_s = 10 \text{ k} - 2 \text{ k} = 8 \text{ k}\Omega$

EXAMPLE 6.6

Finding the voltage gain of an inverting op-amp circuit The parameters of the op-amp circuit in Fig. 6.9 are $R_F = 800 \text{ k}\Omega$, $R_1 = 10 \text{ k}\Omega$, and $A_o = 2 \times 10^5$. Calculate (a) the closed-loop gain $A_f = v_O/v_S$, (b) the output voltage v_O , and (c) the errors in the output voltage v_O and the gain A_f if A_o tends to infinity. Assume that source resistance $R_s = 0$.

SOLUTION

$R_1 = 10 \text{ k}\Omega$, $R_F = 800 \text{ k}\Omega$, $R_F/R_1 = 80$, $A_o = 2 \times 10^5$, and $v_S = 100 \text{ mV}$. From Fig. 6.9, $v_O = A_o v_d$ or $v_d = v_O/A_o$. The input current i_S through R_1 can be found from

$$i_S = \frac{v_S + v_d}{R_1} = \frac{v_S + v_O/A_o}{R_1} \quad (6.19)$$

From Fig. 6.9, the output voltage is given by

$$\begin{aligned} v_O &= -v_d - i_f R_F = -v_d - i_S R_F \quad (\text{since } i_f \approx i_S) \\ &= -\frac{v_O}{A_o} - \frac{v_S + v_O/A_o}{R_1} R_F \end{aligned}$$

which, after simplification, gives the closed-loop voltage gain A_f as

$$A_f = \frac{v_O}{v_S} = -\frac{R_F/R_1}{1 + (1 + R_F/R_1)/A_o} = -\frac{R_F}{R_1(1 + x)} \quad (6.20)$$

$$\text{where} \quad x = \frac{1}{A_o} \left(1 + \frac{R_F}{R_1} \right) \quad (6.21)$$

For a small value of x , which is usually the case, $(1 + x)^{-1} \approx 1 - x$, and Eq. (6.20) can be approximated by

$$A_f = -\frac{R_F}{R_1} (1 - x) \quad (6.22)$$

Therefore, the error introduced for a finite value of gain A_o is x .

(a) From Eq. (6.21),

$$x = (1 + 80)/(2 \times 10^5) = 40.5 \times 10^{-5} = 40.5 \times 10^{-3}\%$$

From Eq. (6.20),

$$A_f = -80/(1 + 40.5 \times 10^{-5}) = -79.9676$$

(b) The output voltage v_O is

$$v_O = A_f v_S = -79.9676 \times 100 \times 10^{-3} = -7.99676 \text{ V}$$

(c) From Eq. (6.22), the error in the output voltage v_O is

$$\Delta v_O = x R_F/R_1 = 40.5 \times 10^{-5} \times 80 = 32.4 \text{ mV, or } 0.0405\%$$

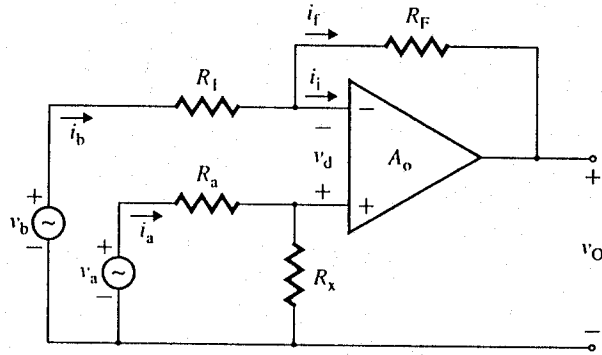
The error in the gain A_f is

$$\Delta A_f = x = 40.5 \times 10^{-5} = 0.0405\%$$

Differential Amplifiers

In the differential amplifier configuration, shown in Fig. 6.10, two input voltages (v_a and v_b) are applied—one to the noninverting terminal and another to the inverting terminal. Resistances R_a and R_x are used to step down the voltage applied to the noninverting terminal. Let us apply the superposition theorem to find the output voltage v_O . That is, we will find the output voltage v_{Oa} , which is due to the input voltage v_a only, and then we will find the output voltage v_{Ob} , which is due to v_b only. The output voltage will be the sum of v_{Oa} and v_{Ob} .

FIGURE 6.10
Differential amplifier



The voltage v_x can be related to the input voltage v_a by

$$v_x = \frac{R_x}{R_x + R_a} v_a \quad (6.23)$$

Applying Eqs. (6.5) and (6.23) gives the output voltage v_{oa} , which is due to the input at the noninverting terminal, as

$$v_{oa} = \left(1 + \frac{R_F}{R_1}\right) v_x = \left(1 + \frac{R_F}{R_1}\right) \left(\frac{R_x}{R_x + R_a}\right) v_a \quad (6.24)$$

Applying Eq. (6.17) gives the output voltage v_{ob} , which is due to the input at the inverting terminal, as

$$v_{ob} = -\frac{R_F}{R_1} v_b \quad (6.25)$$

Therefore, the resultant output voltage is given by

$$v_O = v_{ob} + v_{oa} = -\frac{R_F}{R_1} v_b + \left(1 + \frac{R_F}{R_1}\right) \left(\frac{R_x}{R_x + R_a}\right) v_a \quad (6.26)$$

which, for $R_a = R_1$ and $R_F = R_x$, becomes

$$v_O = (v_a - v_b) \frac{R_F}{R_1} \quad (6.27)$$

Thus, the circuit in Fig. 6.10 can operate as a differential voltage amplifier with a closed-loop voltage gain of R_F/R_1 . For example, if $v_a = 3$ V, $v_b = 5$ V, $R_a = R_1 = 12$ k Ω , and $R_F = R_x = 24$ k Ω , then Eq. (6.27) gives

$$v_O = (3 - 5) \times 24 \text{ k}\Omega / 12 \text{ k}\Omega = -4 \text{ V}$$

If all the resistances have the same values (that is, $R_a = R_1 = R_F = R_x$), Eq. (6.27) is reduced to

$$v_O = v_a - v_b \quad (6.28)$$

in which case the circuit will operate as a difference amplifier. For example if $v_a = 3$ V, $v_b = 5$ V, and $R_a = R_F = R_1 = R_x = 20$ k Ω , then Eq. (6.28) gives

$$v_O = v_a - v_b = 3 - 5 = -2 \text{ V}$$

KEY POINTS OF SECTION 6.4

- Op-amp circuits can be classified into three basic configurations: noninverting, inverting, and differential.

- The output voltage of an op-amp circuit is almost independent of the op-amp parameters; it depends largely on the external circuit elements.
- The analysis of an op-amp circuit can be simplified by assuming that the voltage across the op-amp terminals and the current drawn by the op-amp are very small, tending to zero. The error due to these assumptions generally is less than 0.1%.

6.5 Op-Amp Applications

The applications of op-amps are endless, and there are numerous books on op-amps [1, 2, 4]. Most of the applications are derived from the basic op-amp configurations described in Sec. 6.4. In this section we will discuss several applications of op-amps.

Integrators

If the resistance R_F in the inverting amplifier of Fig. 6.9 is replaced by a capacitance C_F , the circuit will operate as an integrator. Such a circuit is shown in Fig. 6.11(a). R_x is included to minimize the effect of op-amp imperfections (i.e., the input biasing current, which will be discussed in Chapter 7). The value of R_x should be made equal to R_1 . The impedance of C_F in Laplace's domain is $Z_F = 1/(sC_F)$. Applying Eq. (6.17) gives the output voltage in Laplace's domain as

$$V_o(s) = -\left(\frac{Z_F}{Z_1}\right) V_s(s) = -\frac{1}{sR_1C_F} V_s(s) \quad (6.29)$$

from which the output voltage in the time domain becomes

$$v_o(t) = -\frac{1}{R_1C_F} \int_0^t v_s dt + v_C(t=0) \quad (6.30)$$

where $v_C(t=0) = V_{co}$ represents the initial capacitor voltage. That is, the output voltage is given by the integral of the input voltage v_s . Equation (6.30) can also be derived from a circuit analysis similar to that discussed in Sec. 6.4. That is,

$$i_o = i_f = i_s = \frac{v_s + v_d}{R_1} = \frac{v_s}{R_1} \quad (6.31)$$

since the op-amp input current is zero. Therefore, the output voltage, which is the negative of the capacitor voltage, is given by

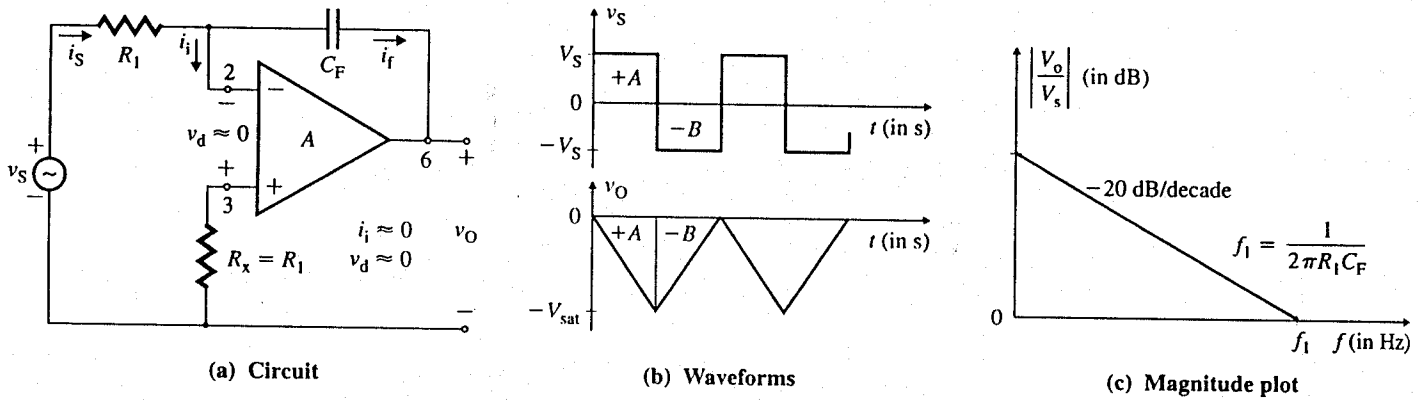
$$v_o(t) = -v_C(t) = -\frac{1}{C_F} \int_0^t i_s dt + v_C(t=0) \quad (6.32)$$

Substituting $i_s = v_s/R_1$ from Eq. (6.31) into Eq. (6.32), we can obtain Eq. (6.30). Time constant $\tau_i = R_1C_F$ for Fig. 6.11(a) is known as the *integration time constant*. If the input is a constant current $i_s = I_s$, then Eq. (6.32) gives

$$v_o(t) = -v_C(t) = -\frac{I_s t}{C_F} + v_C(t=0) = -\frac{Q}{C_F} + v_C(t=0) \quad (6.33)$$

That is, the output voltage is the integral of the input current I_s and is proportional to the input charge Q . Thus, the circuit in Fig. 6.11(a) can also be used as a current integrator, or charge amplifier. The plot of the output voltage for a pulse input is shown in Fig. 6.11(b).

At lower frequencies, the impedance Z_F of C_F will increase, and less signal will be fed back to the inverting terminal of the op-amp. Thus, the output voltage will increase. At

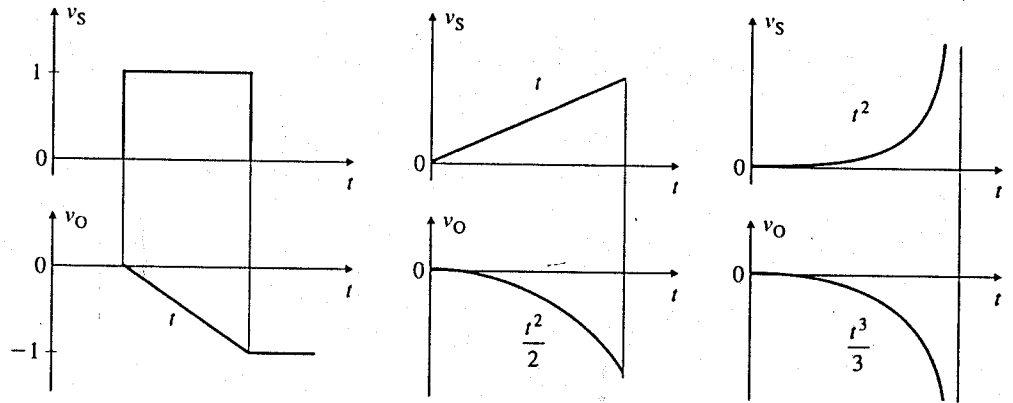
FIGURE 6.11 Integrator circuit

higher frequencies, the impedance Z_F will decrease, causing more signal to be fed back to the inverting terminal. Thus, the output voltage will decrease. Therefore, an integrator circuit behaves like a low-pass filter. The magnitude plot of the voltage gain $V_o(j\omega)/V_s(j\omega)$ in Eq. (6.29) will have a low-pass characteristic with a zero break frequency, as shown in Fig. 6.11(c).

For the case in which the input signal is a constant dc voltage, Eq. (6.30) simplifies to

$$v_O(t) = -\left(\frac{V_S}{R_1 C_F}\right)t + V_{co} \quad (6.34)$$

Typical plots of some input signals and the resulting output signals are shown in Fig. 6.12.

FIGURE 6.12
Typical input and output signals of an integrator

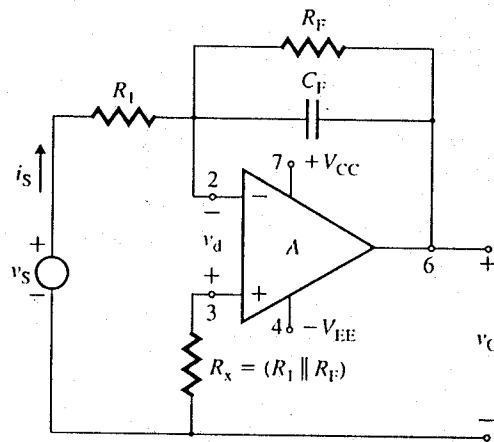
In practice, as a result of its imperfections (e.g., drift, input offset current), an op-amp produces an output voltage even if the input signal is zero ($v_s = 0$), and the capacitor will be charged by the small but finite current through it. The capacitor prevents any dc signal from feeding back from the output terminal to the input side of the op-amp. As a result, the capacitor will be charged continuously, and the output voltage will build up until the op-amp saturates. A resistor with a large value of R_F is normally connected in parallel with the capacitor of capacitance C_F , as shown in Fig. 6.13. R_F provides the dc feedback and overcomes this saturation problem. Time constant $\tau_F (=R_F C_F)$ must be larger than the period $T (=1/f_s)$ of the input signal. A ratio of ten to one is generally adequate; that is, $\tau_F = 10T$. For Fig. 6.13, the feedback impedance is

$$Z_F = R_F \parallel (1/sC_F) = R_F/(1 + sR_F C_F)$$

and Eq. (6.17) gives the output voltage in Laplace's domain as

$$V_o(s) = -\frac{R_F/R_1}{1 + sR_F C_F} V_s(s) \quad (6.35)$$

FIGURE 6.13
Practical inverting
integrator



For a step input voltage of $v_s = V_s$, $V_s(s) = V_s/s$, and Eq. (6.35) can be simplified to give the output voltage in the time domain as

$$v_O(t) = -V_s \frac{R_F}{R_1} (1 - e^{-t/R_F C_F}) \quad (6.36)$$

For $t \leq 0.1 R_F C_F$, Eq. (6.36) can be approximated by

$$v_O(t) = -V_s \frac{R_F}{R_1} \left(\frac{t}{R_F C_F} \right) = - \left(\frac{V_s}{R_1 C_F} \right) t \quad (6.37)$$

which is the time integral of the input voltage. Therefore, the analysis and the input-output relation of the integrator in Fig. 6.11 can be applied to the one in Fig. 6.13, provided $\tau_F \geq 10T$.

EXAMPLE 6.7

D

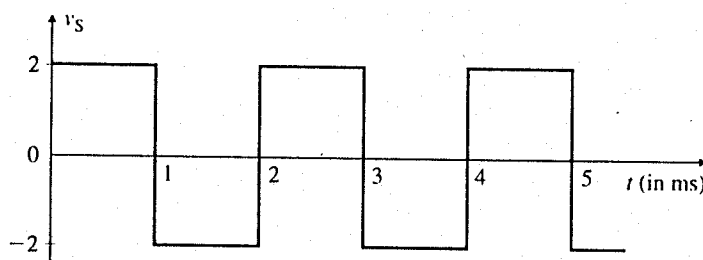
Designing an op-amp integrator

(a) Design an integrator of the form shown in Fig. 6.13. The frequency of the input signal is $f_s = 500$ Hz. The voltage gain should be unity at a frequency of $f_1 = 1590$ kHz. That is, the unity-gain bandwidth is $f_{bw} = 1590$ kHz.

(b) The integrator in part (a) has $V_{CC} = 12$ V, $-V_{EE} = -12$ V, and maximum voltage swing = ± 10 V. The initial capacitor voltage is $V_{co} = 0$ V. Draw the waveform of the output voltage for the input voltage shown in Fig. 6.14.

(c) Use PSpice/SPICE to plot the output voltage for the input voltage in part (b).

FIGURE 6.14 Input voltage for Example 6.7



SOLUTION

(a) The steps in completing the design are as follows.

Step 1. Choose a suitable value of C_F : Let $C_F = 0.1 \mu\text{F}$.

Step 2. Calculate the time constant required to satisfy the unity-gain frequency requirement:

$$\tau_i = \frac{1}{2\pi f_b} = \frac{1}{2\pi \times 1590 \text{ Hz}} = 100 \mu\text{s}$$

Step 3. Calculate the value of R_1 from τ_i :

$$R_1 = \tau_i / C_F = 100 \mu\text{s} / 0.1 \mu\text{F} = 1 \text{ k}\Omega$$

Step 4. Choose time constant $\tau_F = 10T = 10/f_s$:

$$\tau_F = 10/500 \text{ Hz} = 20 \text{ ms}$$

Step 5. Calculate the value of R_F from τ_F :

$$R_F = \tau_F / C_F = 20 \text{ ms} / 0.1 \mu\text{F} = 200 \text{ k}\Omega$$

(b) $V_{\text{sat}} = \pm 10 \text{ V}$, and $\tau_i = R_1 C_F = 1 \times 10^3 \times 0.1 \times 10^{-6} = 0.1 \text{ ms}$. Since $\tau_F \gg \tau_i$, the effect of τ_F can be neglected.

For $0 \leq t \leq 1 \text{ ms}$: From Eq. (6.30), the output voltage is given by

$$v_O = 0 - \frac{1}{R_1 C_F} \int_0^t 2 \, dt = -2 \times 10000t$$

where t is in ms. At $t = 1 \text{ ms}$, $v_O = -20 \text{ V}$, which is more than the saturation voltage and thus is not possible. The time required for the output voltage to reach the saturation voltage of -10 V is $t_1 = 10/(2 \times 10000) = 0.5 \text{ ms}$. For $0.5 \text{ ms} \leq t \leq 1 \text{ ms}$, the capacitor voltage is $V_{\text{co}} = -10 \text{ V}$.

For $1 \text{ ms} \leq t \leq 2 \text{ ms}$: From Eq. (6.30), the output voltage is given by

$$v_O = -10 + \frac{1}{R_1 C_F} \int_0^{t-1} 2 \, dt = -10 + 2 \times 10000(t - 1)$$

where t is in ms. At $t = 2 \text{ ms}$, $v_O = 10 \text{ V}$, and the capacitor voltage is $V_{\text{co}} = 10 \text{ V}$.

For $2 \text{ ms} \leq t \leq 3 \text{ ms}$: From Eq. (6.30), the output voltage is given by

$$v_O = 10 - \frac{1}{R_1 C_F} \int_0^{t-2} 2 \, dt = 10 - 2 \times 10000(t - 2)$$

where t is in ms. At $t = 3 \text{ ms}$, $v_O = -10 \text{ V}$, and the capacitor voltage is $V_{\text{co}} = -10 \text{ V}$.

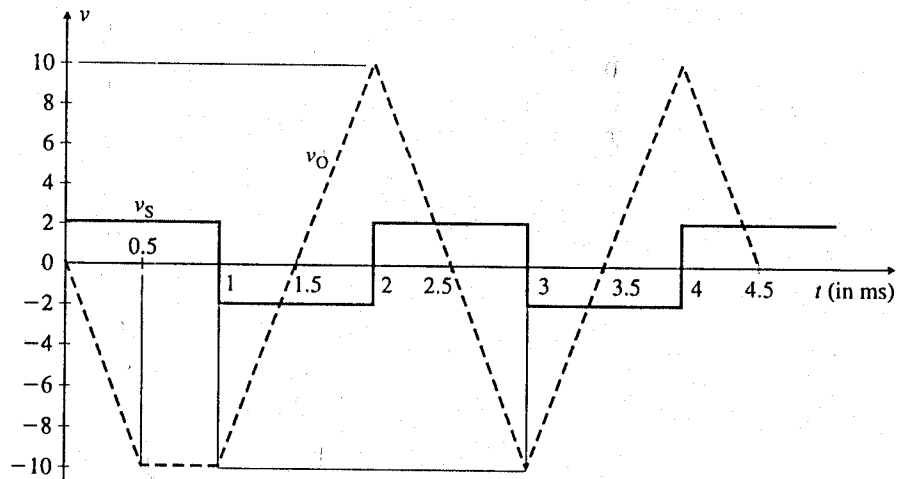
For $3 \text{ ms} \leq t \leq 4 \text{ ms}$: From Eq. (6.30), the output voltage is given by

$$v_O = -10 + \frac{1}{R_1 C_F} \int_0^{t-3} 2 \, dt = -10 + 2 \times 10000(t - 3)$$

where t is in ms. At $t = 4 \text{ ms}$, $v_O = 10 \text{ V}$, and the capacitor voltage is $V_{\text{co}} = 10 \text{ V}$.

The waveforms for input and output voltages are shown in Fig. 6.15.

FIGURE 6.15 Waveforms for Example 6.7



(c) The integrator for PSpice simulation is shown in Fig. 6.16. The list of the circuit file is as follows.

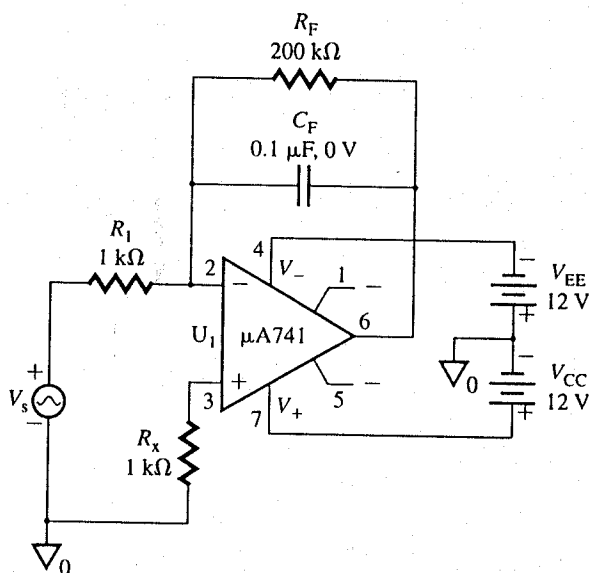
Example 6.7 Practical Integrator

VS 1 0 PULSE (2V -2V 0 1NS 1NS 1MS 2MS) ; Pulse waveform

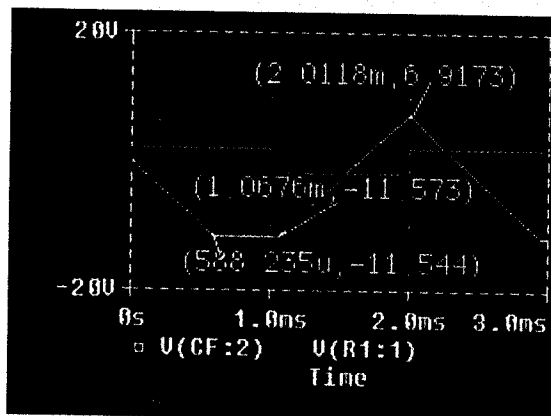
```

CF 3 4 0.1UF
R1 1 3 1K
RF 3 4 200K
RX 2 0 1K
VCC 5 0 DC 12V ; dc positive supply
VEE 0 6 DC 12V ; dc negative supply
.LIB NOM.LIB ; Referring to PSpice library file NOM.LIB
; for UA741 op-amp model
XA1 2 3 5 6 4 UA741 ; Subcircuit call for op-amp UA741
* vi+ vi- +vcc -vee vo
.TRAN 10US 4MS ; Transient analysis
.PROBE ; Graphics post-processor
.END

```

FIGURE 6.16 Integrator circuit for PSpice simulation

The plot of the output voltage $v_O \equiv V(\text{CF}:2)$ is shown in Fig. 6.17. Notice that the results differ significantly from the calculated values, because PSpice uses the characteristics of a real op-amp rather than the ideal model. For example, $t_1 = 0.588$ ms (the expected value is 0.5 ms) and the negative saturation voltage is -11.54 V. The PSpice simulation does not have zener diodes to limit the output to ± 10 V. If zener diodes are connected in the op-amp circuit, the results of the PSpice simulation will be in agreement with the calculated values.

FIGURE 6.17 PSpice plots for Example 6.7

► **NOTE:** While running the PSpice simulation, you must select Use Initial Condition in the setup; otherwise the output plot will be different from what is shown in Fig. 6.17.

EXAMPLE 6.8

Finding the 3-dB frequency of an integrator using Miller's theorem The integrator of Fig. 6.11(a) has $C_F = 0.001 \mu\text{F}$ and $R_1 = 1 \text{ k}\Omega$. The open-loop gain of the op-amp is $A_o = -2 \times 10^5$. Use Miller's theorem (discussed in Section 4.9) to find the 3-dB frequency of the integrator.

SOLUTION

Miller's theorem can be applied to replace the feedback capacitance C_F by an equivalent input capacitance C_x and an output capacitance C_y , as shown in Fig. 6.18. With the open-loop gain $A_o = -A_{vo}$ and the capacitive impedance $Z_F = 1/(j2\pi f C_F)$, we can apply Eqs. (4.95) and (4.98) to find the Miller capacitances:

$$C_x = C_F(1 + A_o) = 0.001 \mu\text{F} \times (1 + 2 \times 10^5) = 200.001 \mu\text{F}$$

$$C_y = C_F(1 + 1/A_o) \approx C_1 = 0.001 \mu\text{F}$$

The output voltage in Laplace's domain is

$$V_o(s) = A_o V_d(s)$$

$$V_d(s) = -\frac{1/(sC_x)}{R_1 + 1/(sC_x)} V_s(s) = -\frac{V_s(s)}{1 + R_1 C_x s}$$

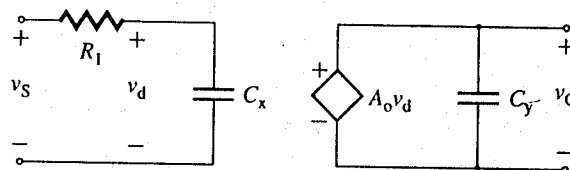
The transfer function between the input and output voltages is given by

$$A(s) = \frac{V_o(s)}{V_s(s)} = -\frac{A_o}{1 + R_1 C_x s}$$

Therefore, the 3-dB frequency is

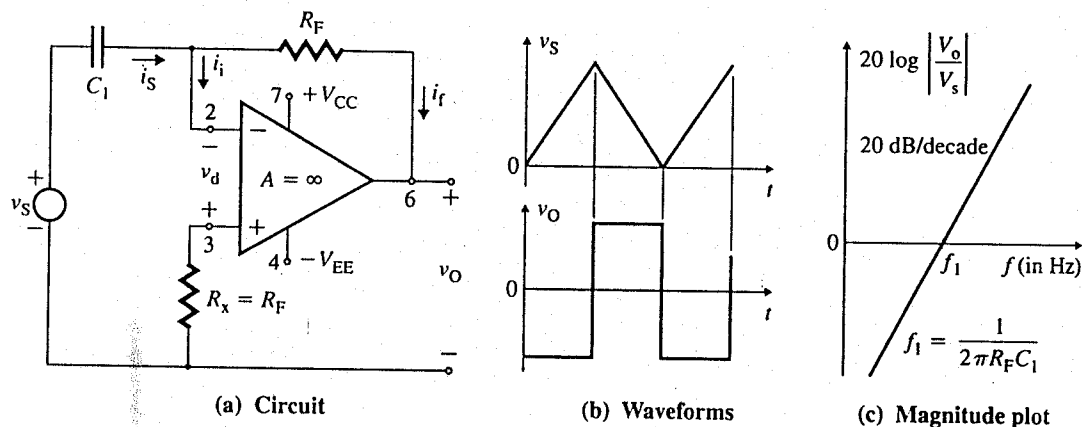
$$\omega_b = 1/(R_1 C_x) = 1/(1 \times 10^3 \times 200.001 \times 10^{-6}) = 5 \text{ rad/s} \quad \text{or} \quad f_b = 0.7958 \text{ Hz}$$

FIGURE 6.18 Equivalent circuit for Example 6.8



Differentiators

FIGURE 6.19
Differentiator circuit



If the resistance R_1 in the inverting amplifier of Fig. 6.9 is replaced by a capacitance C_1 , as shown in Fig. 6.19(a), the circuit will operate as a differentiator. The value of R_x should

be made equal to R_F . The impedance of C_1 in Laplace's transform is $Z_1 = 1/(sC_1)$. Using Eq. (6.17), we can find the output voltage in Laplace's domain as

$$V_o(s) = -\left(\frac{R_F}{Z_1}\right)V_s(s) = -sR_FC_1V_s(s) \quad (6.38)$$

which gives the output voltage in the time domain as

$$v_O = -R_FC_1 \frac{dv_S}{dt} \quad (6.39)$$

This equation can also be derived from a circuit analysis similar to that discussed in Sec. 6.4. That is,

$$i_S = i_f = C_1 \frac{dv_S}{dt} \quad (6.40)$$

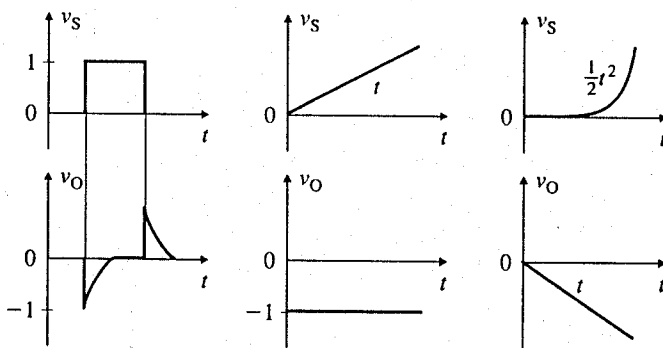
$$v_O = -R_F i_f = -R_F i_S \quad (6.41)$$

Substituting i_S from Eq. (6.40) into Eq. (6.41) gives Eq. (6.39). Time constant $\tau_d = R_FC_1$ in Fig. 6.19(a) is known as the *differentiator time constant*. The output voltage in response to a triangular wave is shown in Fig. 6.19(b).

A differentiator circuit is useful in producing sharp trigger pulses to drive other circuits. When the frequency is increased, the impedance Z_1 of C_1 decreases and the output voltage increases. Therefore, a differentiator circuit behaves like a high-pass network. The magnitude plot of the voltage gain $V_o(j\omega)/V_s(j\omega)$ in Eq. (6.38) has a high-pass characteristic with an infinite break frequency, as shown in Fig. 6.19(c). Typical plots of some input signals and the resulting output signals are shown in Fig. 6.20.

FIGURE 6.20

Typical input and output signals of a differentiator



If there is any sharp change in the input voltage $v_S(t)$ due to noise or picked-up interference, there will be amplified spikes at the output, and the circuit will behave like a noise magnifier. Thus, this type of differentiating circuit is not often used. A modified circuit that is often utilized as a differentiator is shown in Fig. 6.21(a), in which a small resistance R_1 ($< R_F$) is connected in series with C_1 to limit the gain at high frequencies. However, this arrangement also limits the high-frequency range, as shown in the magnitude plot in Fig. 6.21(b).

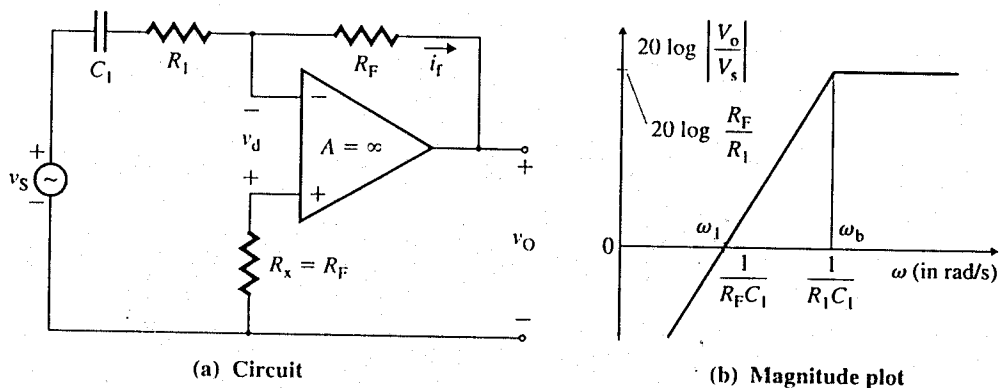
The impedance Z_1 for R_1 and C_1 in Laplace's domain is

$$Z_1 = R_1 + \frac{1}{sC_1} = \frac{1 + sR_1C_1}{sC_1}$$

Using Eq. (6.38), we have for the transfer function of the circuit in Fig. 6.21(a)

$$A_f(s) = \frac{V_o(s)}{V_s(s)} = -\frac{R_F}{Z_1} = -\frac{R_FC_1s}{1 + sR_1C_1} \quad (6.42)$$

FIGURE 6.21
Practical inverting
differentiator



For $s = j\omega$,

$$A_f(j\omega) = -\frac{R_F C_1 j\omega}{1 + j\omega R_1 C_1} \quad (6.43)$$

The magnitude of Eq. (6.43) is given by

$$|A_f(j\omega)| = \frac{R_F C_1 \omega}{[1 + (\omega R_1 C_1)^2]^{1/2}} \quad (6.44)$$

Therefore, the break frequency is $\omega_b = 1/(R_1 C_1)$. For frequencies greater than ω_b , $(\omega R_1 C_1)^2 \gg 1$, and Eq. (6.44) reduces to

$$|A_f(j\omega)| = \frac{R_F}{R_1} \quad (6.45)$$

EXAMPLE 6.9

D

Designing an op-amp differentiator

(a) Design a differentiator of the form shown in Fig. 6.21(a) to satisfy the following specifications: gain-limiting frequency $f_b = 1$ kHz, and maximum closed-loop gain $A_{f(\max)} = 10$. Determine the values of R_1 , R_F , and C_1 .

(b) Use PSpice/SPICE to plot the frequency response for part (a). Assume a sinusoidal input voltage of peak value $v_{S(\text{peak})} = 0.1$ V.

SOLUTION

$A_{f(\max)} = 10$, and $f_b = 1$ kHz.

(a) The steps in completing the design are as follows.

Step 1. Choose a suitable value for capacitance C_1 : Let $C_1 = 0.1 \mu\text{F}$.

Step 2. Calculate the value of R_1 from the break frequency f_b :

$$\begin{aligned} f_b &= 1/(2\pi R_1 C_1) \\ 1 \text{ kHz} &= 1/(2\pi R_1 \times 0.1 \times 10^{-6}) \\ R_1 &= 1592 \Omega \end{aligned}$$

Step 3. Calculate the value of R_F from Eq. (6.45):

$$\begin{aligned} A_{f(\max)} &= R_F/R_1 \\ R_F &= 1592 A_{f(\max)} = 1592 \times 10 = 15.92 \text{ k}\Omega \end{aligned}$$

(b) The differentiator circuit for PSpice simulation is shown in Fig. 6.22. The list of the circuit file is as follows.

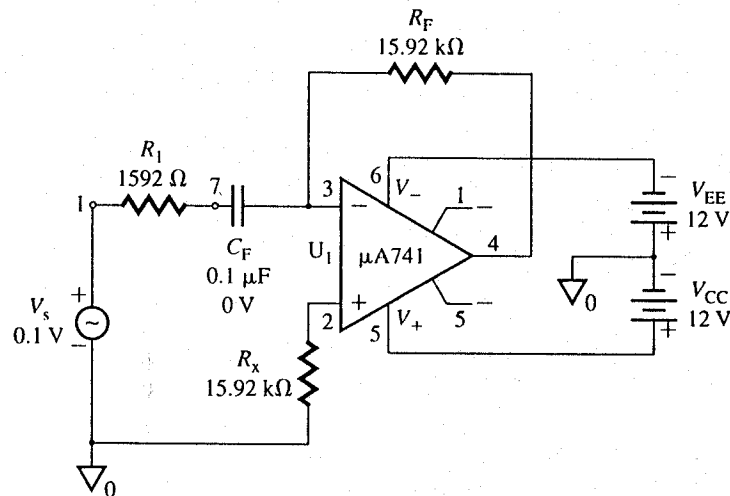
Example 6.9 Differentiator

```
VI 1 0 AC 0.1V ; ac voltage of 1 V (peak)
R1 1 7 1592
```

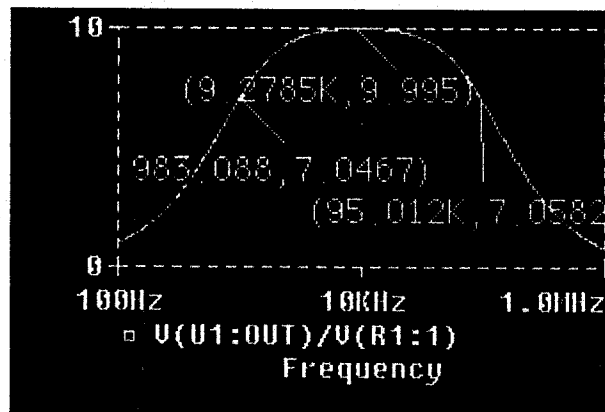
```

C1 7 3 0.1UF
RF 3 4 15.92K
RX 2 0 15.92K
VCC 5 0 DC 12V ; dc positive supply
VEE 0 6 DC 12V ; dc negative supply
.LIB NOM.LIB ; Referring to PSpice library file NOM.LIB
; for UA741 op-amp model
XA1 2 3 5 6 4 UA741 ; Subcircuit call for op-amp UA741
* vi+ vi- +vcc -vee vo
.AC DEC 10 100HZ 1MEGHZ ; ac analysis
.PROBE ; Graphics post-processor
.END

```

FIGURE 6.22 Differentiator circuit for PSpice simulation

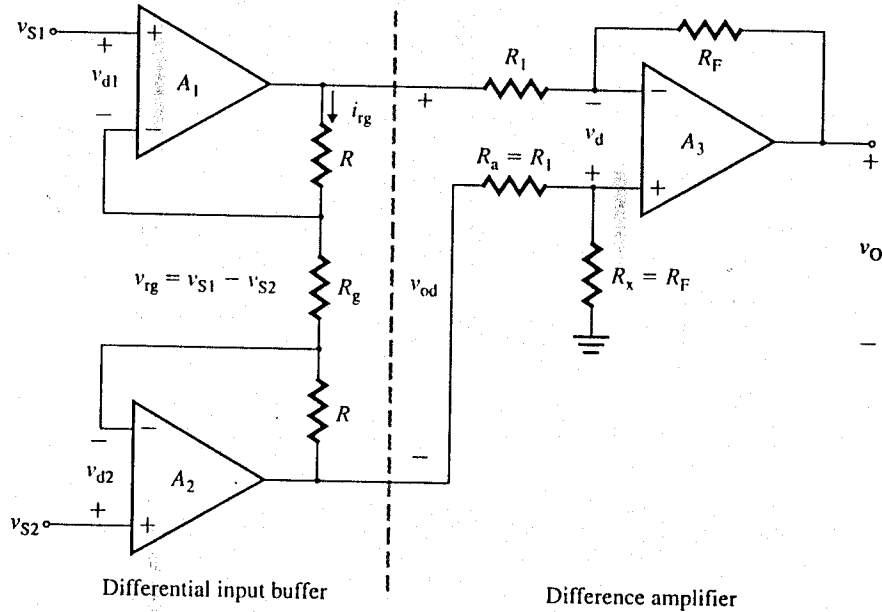
The plot of the frequency response for the output voltage is shown in Fig. 6.23, which gives $A_{f(\max)} = 9.995$ (expected value is $100 \times 0.1 = 10$). The break frequency f_b (at $A_f = 9.995 \times 0.707 = 7.07$) is 983 Hz (expected value is 1 kHz). The upper frequency limit (that is, 95 kHz) is due to the internal frequency behavior of the op-amp.

FIGURE 6.23 PSpice plot for Example 6.9

An instrumentation amplifier is a dedicated differential amplifier with an extremely high input impedance. Its gain can be precisely set by a single resistance. It has a high common-mode rejection capability (i.e., it is able to reject a signal that is common to both terminals but to amplify a differential signal), and this feature is very useful for receiving small

signals buried in large common-mode offsets or noise. Therefore, instrumentation amplifiers are commonly used as signal conditioners of low-level (often dc) signals in large amounts of noise. The circuit diagram of an instrumentation amplifier is shown in Fig. 6.24. The amplifier consists of two stages. The first stage is the differential stage. Each input signal (v_{S1} or v_{S2}) is applied directly to the noninverting terminal of its op-amp in order to provide the very high input impedance. The second stage is a difference amplifier, which gives a low output impedance and can also allow voltage gain.

FIGURE 6.24
Instrumentation amplifier



The voltage drop between the input terminals of an op-amp is very small, tending to zero: $v_{d1} = v_{d2} = 0$. Thus, the voltage drop across the middle resistor R_g of the potential divider is

$$v_{rg} = v_{S1} - v_{S2}$$

which gives the current i_{rg} through R_g as

$$i_{rg} = \frac{v_{rg}}{R_g} = \frac{v_{S1} - v_{S2}}{R_g}$$

This current flows through all three of the resistors, because the currents flowing into the input terminals of the op-amps are zero. Therefore, the output voltage of the differential stage becomes

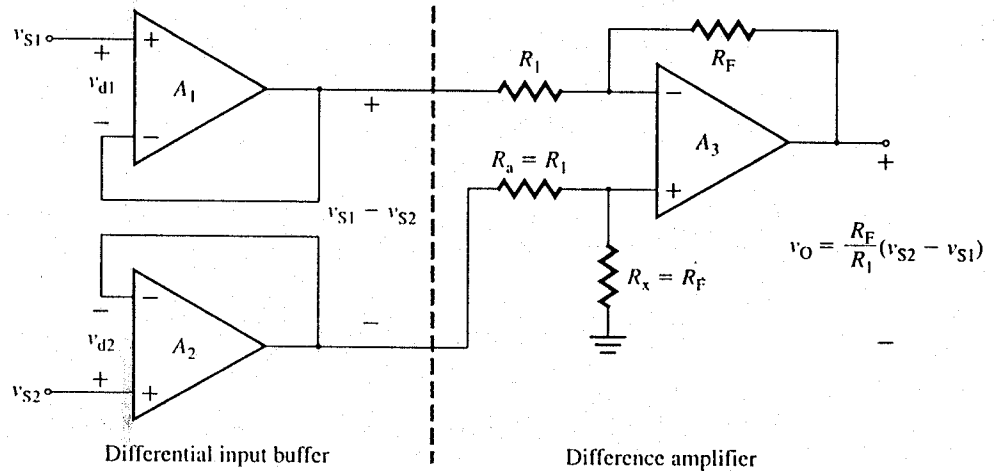
$$v_{od} = i_{rg}(R_g + 2R) = \frac{v_{S1} - v_{S2}}{R_g}(R_g + 2R) = (v_{S1} - v_{S2})\left(1 + \frac{2R}{R_g}\right)$$

Using Eq. (6.27), we can calculate the output voltage v_O as

$$v_O = -v_{od} \frac{R_F}{R_1} = -(v_{S1} - v_{S2})\left(1 + \frac{2R}{R_g}\right)\left(\frac{R_F}{R_1}\right) \quad (6.46)$$

which is the output of the instrumentation amplifier. This gain is normally varied by R_g . If the gain variation is not desired, then R_g can be removed and the difference amplifier can be made with two unity-gain voltage followers. This arrangement is shown in Fig. 6.25.

FIGURE 6.25
Instrumentation amplifier
with fixed gain



Noninverting Summing Amplifiers

The basic noninverting amplifier in Fig. 6.7 can be operated as a summing amplifier. A noninverting summing amplifier with three inputs is shown in Figure 6.26. Summing amplifiers are commonly employed in analog computing. By the superposition theorem, the voltage v_n at the noninverting terminal is

$$\begin{aligned} v_n &= \frac{R_b \parallel R_c}{R_a + R_b \parallel R_c} v_a + \frac{R_a \parallel R_c}{R_b + R_a \parallel R_c} v_b + \frac{R_a \parallel R_b}{R_c + R_a \parallel R_b} v_c \\ &= \frac{R_A}{R_a} v_a + \frac{R_A}{R_b} v_b + \frac{R_A}{R_c} v_c \end{aligned} \quad (6.47)$$

$$\text{where } R_A = (R_a \parallel R_b \parallel R_c) \quad (6.48)$$

Applying Eq. (6.5) for the noninverting amplifier and Eq. (6.47) gives the output voltage:

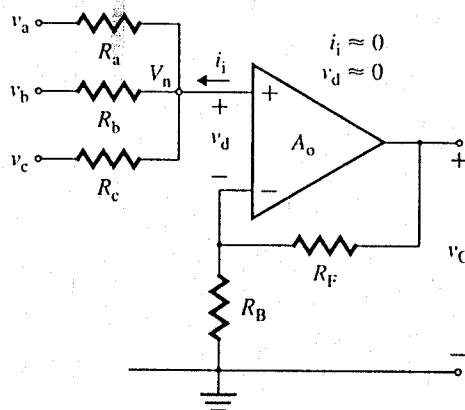
$$v_O = \left(1 + \frac{R_F}{R_B}\right) v_n = \left(1 + \frac{R_F}{R_B}\right) \left(\frac{R_A}{R_a} v_a + \frac{R_A}{R_b} v_b + \frac{R_A}{R_c} v_c\right) \quad (6.49)$$

For $R_a = R_b = R_c = R$, Eq. (6.48) gives $R_A = R/3$, and Eq. (6.49) becomes

$$v_O = \left(1 + \frac{R_F}{R_B}\right) \left(\frac{v_a + v_b + v_c}{3}\right) \quad (6.50)$$

Thus, the output voltage is equal to the average of all the input voltages times the closed-loop gain $(1 + R_F/R_B)$ of the circuit. If the circuit is operated as a unity follower with

FIGURE 6.26
Noninverting summing
amplifier



$R_F = 0$ and $R_B = \infty$, the output voltage will be equal to the average of all the input voltages. That is,

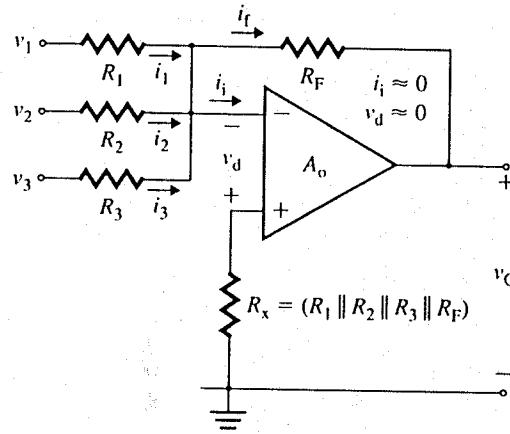
$$v_O = \frac{v_a + v_b + v_c}{3} \quad (6.51)$$

If the closed-loop gain $(1 + R_F/R_B)$ is made equal to the number of inputs, the output voltage becomes equal to the sum of all the input voltages. That is, for three inputs, $n = 3$, and $(1 + R_F/R_B) = n = 3$. Then, Eq. (6.50) becomes

$$v_O = v_a + v_b + v_c \quad (6.52)$$

Inverting Summing Amplifiers

FIGURE 6.27
Inverting summing amplifier



The value of R_x should equal the parallel combination of R_1 , R_2 , R_3 , and R_F . That is,

$$R_x = (R_1 \parallel R_2 \parallel R_3 \parallel R_F) \quad (6.53)$$

For an ideal op-amp, $v_d \approx 0$. Using Ohm's law, we get

$$i_1 = \frac{v_1}{R_1}, \quad i_2 = \frac{v_2}{R_2}, \quad i_3 = \frac{v_3}{R_3}, \quad i_f = -\frac{v_O}{R_F}$$

Since the current flowing into the op-amp is zero ($i_i = 0$),

$$i_1 + i_2 + i_3 = i_f$$

$$\text{or} \quad \frac{v_1}{R_1} + \frac{v_2}{R_2} + \frac{v_3}{R_3} = -\frac{v_O}{R_F} \quad (6.54)$$

which gives the output voltage as

$$v_O = -\left(\frac{R_F}{R_1} v_1 + \frac{R_F}{R_2} v_2 + \frac{R_F}{R_3} v_3\right) \quad (6.55)$$

Thus, v_O is a weighted sum of the input voltages, and this circuit is also called a *weighted*, or *scaling*, *summer*. If $R_1 = R_2 = R_3 = R_F = R$, Eq. (6.55) is reduced to

$$v_O = -(v_1 + v_2 + v_3) \quad (6.56)$$

and the circuit becomes a summing amplifier. If $R_1 = R_2 = R_3 = nR_F$, where n is the number of input signals, the circuit operates as an averaging amplifier. For three inputs, $n = 3$, and Eq. (6.55) becomes

$$v_O = -\frac{v_1 + v_2 + v_3}{3} \quad (6.57)$$

Addition-Subtraction Amplifiers

The functions of noninverting and inverting summing amplifiers can be implemented by only one op-amp, as shown in Fig. 6.28, in order to give output voltage of the form

$$v_O = A_1 v_a + A_2 v_b + A_3 v_c - B_1 v_1 - B_2 v_2 - B_3 v_3$$

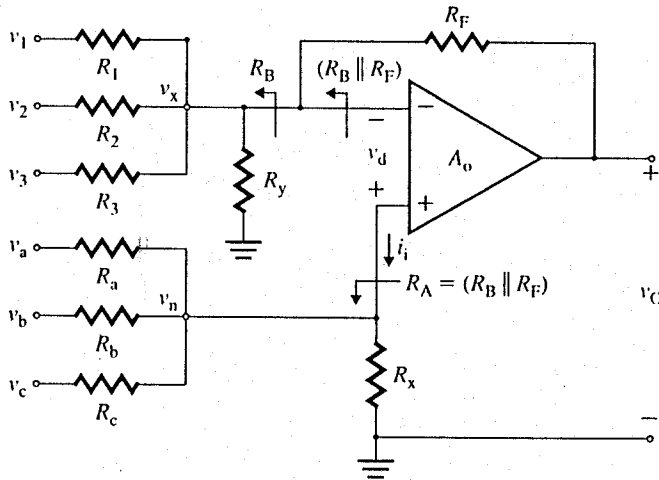
where A_1, A_2, A_3, B_1, B_2 , and B_3 are the gain constants. The resistances R_x and R_y are included to make the configuration more general. Applying Eqs. (6.49) and (6.55) gives an expression for the resultant output voltage:

$$v_O = \left(1 + \frac{R_F}{R_B}\right) \left(\frac{R_A}{R_a} v_a + \frac{R_A}{R_b} v_b + \frac{R_A}{R_c} v_c \right) - \left(\frac{R_F}{R_1} v_1 + \frac{R_F}{R_2} v_2 + \frac{R_F}{R_3} v_3 \right) \quad (6.58)$$

$$\text{where } R_A = (R_a \parallel R_b \parallel R_c \parallel R_x) \quad (6.59)$$

$$R_B = (R_1 \parallel R_2 \parallel R_3 \parallel R_y) \quad (6.60)$$

FIGURE 6.28
Addition-subtraction amplifier



To minimize the effects of offset biasing currents on the output of op-amps (discussed further in Chapter 7), Thevenin's equivalent resistance looking from the noninverting terminal is normally made equal to that looking from the inverting terminal. That is,

$$(R_B \parallel R_F) = R_A \quad (6.61)$$

$$\text{or } \frac{R_B R_F}{R_B + R_F} = R_A$$

Using this condition, we can simplify the term $(1 + R_F/R_B)R_A$:

$$\left(1 + \frac{R_F}{R_B}\right)R_A = \left(1 + \frac{R_F}{R_B}\right)\left(\frac{R_B R_F}{R_B + R_F}\right) = R_F$$

Substituting this relation into Eq. (6.58) yields

$$v_O = \left(\frac{R_F}{R_a} v_a + \frac{R_F}{R_b} v_b + \frac{R_F}{R_c} v_c \right) - \left(\frac{R_F}{R_1} v_1 + \frac{R_F}{R_2} v_2 + \frac{R_F}{R_3} v_3 \right) \quad (6.62)$$

which has the general form

$$v_O = A_1 v_a + A_2 v_b + A_3 v_c - B_1 v_1 - B_2 v_2 - B_3 v_3$$

Equation (6.62) is valid only if the condition of Eq. (6.61) is satisfied. For known values of gain constants A and B , the resistance values can be determined. Difficulty arises, however, in determining values of R_x and R_y that meet the criteria of Eq. (6.61). A technique proposed by W. P. Vrbancic [4] can be applied to determine the values of R_x and R_y . If details and proof of this technique are omitted, the design procedures can be simplified to the following steps:

Step 1. Add all the positive coefficients: $A = A_1 + A_2 + A_3$.

Step 2. Add all the negative coefficients: $B = B_1 + B_2 + B_3$.

Step 3. Define a parameter $C = A - B - 1$.

Step 4. Depending on the value of C , determine the values of R_x and R_y :

- If $C > 0$, $R_x = \infty$ and $R_y = R_F/C$.
- If $C < 0$, $R_x = -R_F/C$ and $R_y = \infty$.
- If $C = 0$, $R_x = \infty$ and $R_y = \infty$.

Step 5. Choose a suitable value of R_F , and find the values of the other components. R_F is normally chosen to meet one of the following constraints:

- If the equivalent resistance R_A is to be set to a particular value, R_F can be found from the relation $R_F = MR_A$, where M is the largest value of A , or $(B + 1)$.
- If the minimum value of any resistances is to be limited to $R_{\min}$, R_F can be found from the relation $R_F = NR_{\min}$, where N is the largest value of $A_1, A_2, A_3, B_1, B_2, B_3$, or C .

(If it is not necessary to meet any of these conditions, the design can be completed by choosing a suitable value of R_F .)

Step 6. If the value of any resistor is too high or too low, you can multiply all the resistances by a constant without affecting the output voltage or the condition of Eq. (6.61).

EXAMPLE 6.10

D

Designing a summing op-amp circuit for a certain resistance R_A Design an inverting and a non-inverting summing amplifier of the configuration shown in Fig. 6.28 to give an output voltage of the form

$$v_O = 4v_a + 6v_b + 3v_c - 7v_1 - v_2 - 5v_3$$

The equivalent resistance R_A is to be set to 15 k Ω .

SOLUTION

The coefficients are $A_1 = 4$, $A_2 = 6$, $A_3 = 3$, $B_1 = 7$, $B_2 = 1$, and $B_3 = 5$. Let us follow the design steps described above.

Step 1. $A = 4 + 6 + 3 = 13$.

Step 2. $B = 7 + 1 + 5 = 13$.

Step 3. $C = A - B - 1 = 13 - 13 - 1 = -1$.

Step 4. Since $C < 0$, $R_x = -R_F/C = R_F$ and $R_y = \infty$.

Step 5. The design can be completed by choosing a value of R_F . For the given value of $R_A = 15$ k Ω , $R_F = MR_A$. In this case, $M = B + 1 = 13 + 1 = 14$. Thus, the values are as follows:

$$R_F = R_y = MR_B = 14 \times 15 = 210 \text{ k}\Omega$$

$$R_a = R_F/A_1 = 210 \text{ k}/4 = 52.5 \text{ k}\Omega$$

$$R_b = R_F/A_2 = 210 \text{ k}/6 = 35 \text{ k}\Omega$$

$$R_c = R_F/A_3 = 210 \text{ k}/3 = 70 \text{ k}\Omega$$

$$R_x = -R_F/C = 210 \text{ k}\Omega$$

$$R_1 = R_F/B_1 = 210 \text{ k}/7 = 30 \text{ k}\Omega$$

$$R_2 = R_F/B_2 = 210 \text{ k}/1 = 210 \text{ k}\Omega$$

$$R_3 = R_F/B_3 = 210 \text{ k}/5 = 42 \text{ k}\Omega$$

$$R_y = \infty$$

Check:

From Eq. (6.59),

$$R_A = (52.5 \text{ k}\Omega \parallel 35 \text{ k}\Omega \parallel 70 \text{ k}\Omega \parallel 210 \text{ k}\Omega) = 15 \text{ k}\Omega$$

From Eq. (6.60),

$$R_B = (30 \text{ k}\Omega \parallel 210 \text{ k}\Omega \parallel 42 \text{ k}\Omega) = 16.15 \text{ k}\Omega$$

From Eq. (6.61),

$$R_B \parallel R_F = (16.15 \text{ k}\Omega \parallel 210 \text{ k}\Omega) = 15 \text{ k}\Omega$$

Thus, the condition of $R_A = (R_B \parallel R_F)$ is satisfied.

EXAMPLE 6.11

D

Designing a summing op-amp circuit for a minimum resistance $R_{\min}$ Design an inverting and a noninverting summing amplifier of the configuration shown in Fig. 6.28 to give an output voltage of the form

$$v_O = 8v_a + 6v_b + 3v_c - 7v_1 - v_2 - 5v_3$$

The minimum value of any resistance is to be set to $R_{\min} = 15 \text{ k}\Omega$.

SOLUTION

The coefficients are $A_1 = 8$, $A_2 = 6$, $A_3 = 3$, $B_1 = 7$, $B_2 = 1$, and $B_3 = 5$. Let us follow the design steps described earlier.

Step 1. $A = 8 + 6 + 3 = 17$.

Step 2. $B = 7 + 1 + 5 = 13$.

Step 3. $C = A - B - 1 = 17 - 13 - 1 = 3$.

Step 4. Since $C > 0$, $R_x = \infty$ and $R_y = R_F/C = R_F/3$.

Step 5. The design can be completed by choosing a value of R_F . For the given value of $R_{\min} = 15 \text{ k}\Omega$, $R_F = NR_{\min}$, where N is the largest value of A_1 , A_2 , A_3 , B_1 , B_2 , B_3 , or C . In this case, $N = 8$. Thus, the values are as follows:

$$R_F = NR_{\min} = 8 \times 15 \text{ k} = 120 \text{ k}\Omega$$

$$R_a = R_F/A_1 = 120 \text{ k}/8 = 15 \text{ k}\Omega$$

$$R_b = R_F/A_2 = 120 \text{ k}/6 = 20 \text{ k}\Omega$$

$$R_c = R_F/A_3 = 120 \text{ k}/3 = 40 \text{ k}\Omega$$

$$R_x = \infty$$

$$R_1 = R_F/B_1 = 120 \text{ k}/7 = 17.14 \text{ k}\Omega$$

$$R_2 = R_F/B_2 = 120 \text{ k}/1 = 120 \text{ k}\Omega$$

$$R_3 = R_F/B_3 = 120 \text{ k}/5 = 24 \text{ k}\Omega$$

$$R_y = R_F/C = 120 \text{ k}/3 = 40 \text{ k}\Omega$$

Check:

From Eq. (6.59),

$$R_A = (15 \text{ k}\Omega \parallel 20 \text{ k}\Omega \parallel 40 \text{ k}\Omega) = 7.06 \text{ k}\Omega$$

From Eq. (6.60),

$$R_B = (17.14 \text{ k}\Omega \parallel 120 \text{ k}\Omega \parallel 24 \text{ k}\Omega \parallel 40 \text{ k}\Omega) = 7.5 \text{ k}\Omega$$

From Eq. (6.61),

$$R_B \parallel R_F = (7.5 \text{ k}\Omega \parallel 120 \text{ k}\Omega) = 7.06 \text{ k}\Omega$$

Thus, the condition of $R_A = (R_B \parallel R_F)$ is satisfied.

Optocoupler Drivers

Optocouplers, also known *optical isolators*, are generally used to transfer electrical signals from one part of a system to another without direct electrical connection. They find many applications in instrumentation for electrical power engineering, where direct electrical connections between low-level signals and high-current power lines must be avoided, and in medical electronics, where direct connections between patients and electrical power systems must be avoided.

An optocoupler consists of a light-emitting diode (LED), which emits light when forward current is applied, and a photodiode, which converts light to electrical current proportional to the incident light. The light power produced by an LED is directly proportional to the current through the diode. However, the output power is a nonlinear function of the diode voltage. Therefore, an optocoupler is supplied by a current source.

A optocoupler drive circuit is shown in Fig. 6.29. This circuit is a modification of the inverting op-amp shown in Fig. 6.9. Since the current flowing through the op-amp is very small, tending to zero, $i_S = i_f$. Thus, the voltage across R_2 is

$$v_O = -R_F i_f = -R_F i_S$$

The load current i_O is given by

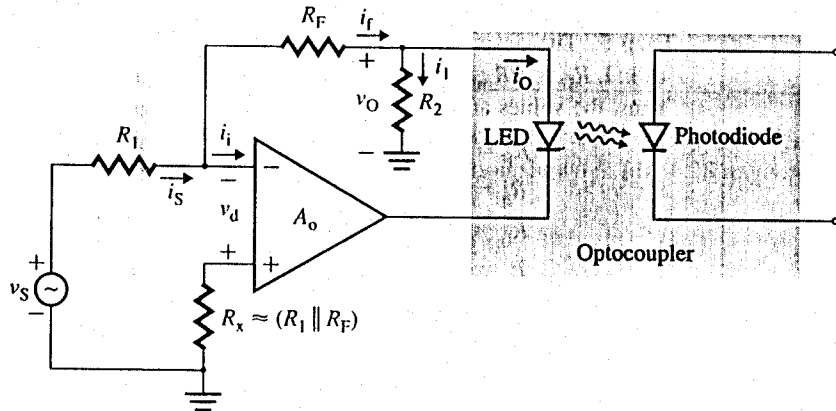
$$i_O = i_f - i_1 = i_S + \frac{R_F i_S}{R_2} = \left(1 + \frac{R_F}{R_2}\right) i_S \quad (6.63)$$

Therefore, the circuit operates as a current amplifier. The LED acting as the load does not determine the load current i_O . Only the multiplier R_F/R_2 determines the load current. Substituting $i_S \approx v_S/R_1$ gives the output current as a function of the input voltage. That is,

$$i_O = \left(1 + \frac{R_F}{R_2}\right) \left(\frac{1}{R_1}\right) v_S \quad (6.64)$$

The circuit then operates as a transconductance amplifier (or voltage-current converter).

FIGURE 6.29
Optocoupler drive circuit

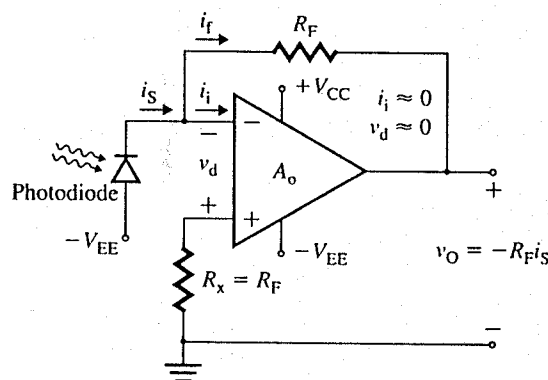


Photodetectors

A photodiode produces a current that is a linear function of the light intensity; this current is normally measured as incident optical power density D_p . The ratio of the output current to the incident optical power density is called the *current responsivity*. This current can be measured by an inverting op-amp of the type shown in Fig. 6.9, which is a current-voltage converter. The output voltage depends on the input current. From Eq. (6.15) for $v_d = 0$, we get

$$v_O = -R_F i_f = -R_F i_S$$

A simple light-sensing circuit consisting of a photodiode and an inverting op-amp is shown in Fig. 6.30. The anode terminal of the diode can be connected to either the ground or a negative voltage. However, a reverse-biasing voltage will reduce the diode junction capacitance, which in turn decreases the frequency (or transient) response time of the circuit.

FIGURE 6.30
Photodetector circuit**EXAMPLE 6.12****D****SOLUTION**

Designing an op-amp photodetector circuit Design a photodetector circuit of the form shown in Fig. 6.30 to give an output voltage of -200 mV at an incident power density of $D_p = 500$ nW/cm². The current responsivity of the photodiode is $D_i = 1$ A/W, and the active area is $a = 40$ mm².

The power produced by the photodiode is

$$P = D_p a = (500 \text{ nW/cm}^2) \times 40 \text{ mm}^2 = 200 \text{ nW}$$

Therefore, the current produced by the diode is

$$i_S = PD_i = 1 \text{ A/W} \times 200 \text{ nW} = 200 \text{ nA}$$

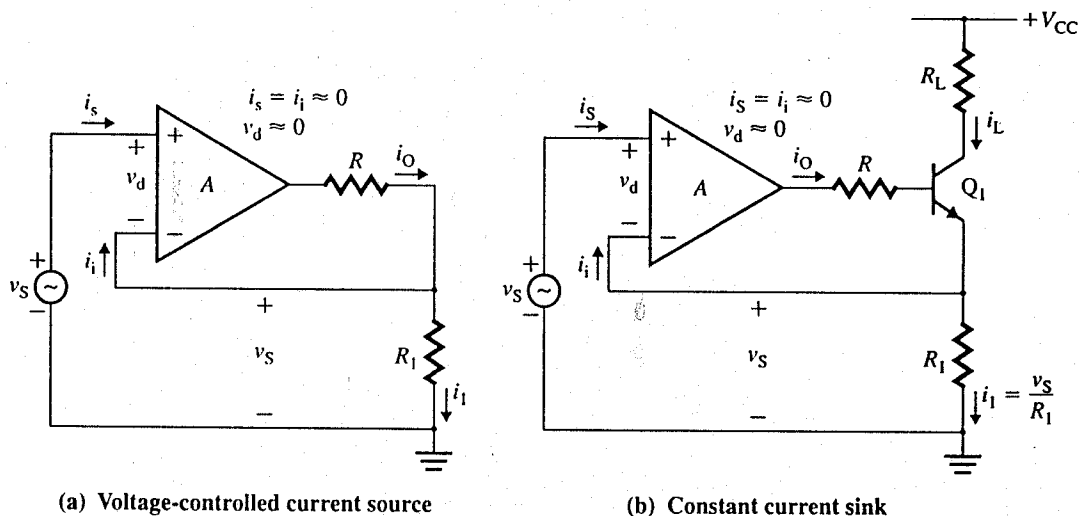
The output voltage is $v_O = -R_F i_S$, which, for $i_S = 200$ nA and $v_O = -200$ mV, gives

$$R_F = -v_O / i_S = 200 \text{ mV} / 200 \text{ nA} = 1 \text{ M}\Omega$$

Voltage-Current Converters

If the input signal is a voltage source and it is transmitted to a remote load, the load current will depend on the series resistance between the input signal and the load. Even a small drop across the series resistance could significantly change the percentage error of the load voltage. Any changes in the load resistance due to wear and tear or temperature will contribute to the error. The simplest type of voltage-current converter, shown in Fig. 6.31(a), is a modification of the basic noninverting amplifier shown in Fig. 6.7(a). The current through the resistor R_1 is given by

$$i_O = i_1 = \frac{v_S - v_d}{R_1} = \frac{v_S}{R_1} \quad (6.65)$$

FIGURE 6.31
Voltage-current converter

(a) Voltage-controlled current source

(b) Constant current sink

Thus, the output current i_O through the load resistance R depends only on v_S and R_1 , not on R . For a fixed value of R_1 , i_O is directly proportional to v_S . Note that none of the load terminals in Fig. 6.31(a) is connected to the ground. That is, the load is floating. The advantage of this arrangement is that no common-mode signal (i.e., noise) will appear across the load.

Op-amps are primarily voltage amplifiers; their current-carrying capability is very limited. Many applications (such as indicators and actuators) require regulated variable current, which is beyond the op-amp's capability. The circuit shown in Fig. 6.31(b) can provide the load current i_L proportional to the input voltage v_S . The output of the op-amp forces the base current through transistor Q_1 , resulting in a proportional collector current through Q_1 , the load R_L , and R_1 . The load current i_L can be controlled by varying either the input voltage or the value of R_1 . The value of the base resistance R must be sufficiently large to protect the base-emitter junction of Q_1 and to limit the output current of the op-amp. Also, the dc supply voltage $V_{CC} \geq R_L i_L (\approx v_S R_L / R_1)$. The load resistance R_L is floating. Thus, the circuit cannot be used with a grounded load.

dc Voltmeters

The voltage-current converter in Fig. 6.31(a), which consists of a noninverting amplifier, can be used as a dc voltmeter, as shown in Fig. 6.32. Since all signals are dc quantities, we will use uppercase symbols. A moving coil meter with an internal resistance of R_m is connected in the feedback path. For an ideal op-amp, $v_d \approx 0$; the meter current is given by

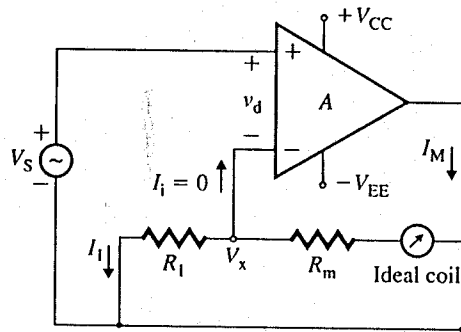
$$I_M = I_1 = \frac{V_X}{R_1} = \frac{V_S + v_d}{R_1} = \frac{V_S}{R_1} \quad (6.66)$$

which gives the relation between the input voltage and the meter current as

$$V_S = R_1 I_M \quad (6.67)$$

Thus, the input voltage V_S can be measured from the deflection of the meter, which is proportional to I_M . If the full-scale deflection current of the moving coil is $I_{M(\max)} = 100 \mu\text{A}$ and $R_1 = 2 \text{ M}\Omega$, the full-scale reading will be $V_{S(\max)} = R_1 I_{M(\max)} = 2 \text{ M}\Omega \times 100 \mu\text{A} = 200 \text{ V}$.

FIGURE 6.32
dc voltmeter



dc Millivoltmeters

The inverting amplifier in Fig. 6.9 can be operated as a dc millivoltmeter, as shown in Fig. 6.33. This circuit is similar to the optocoupler drive in Fig. 6.29, except that the LED is shorted, and we expect similar equations. As before, we will use uppercase symbols for dc quantities. For an ideal amplifier, $v_d = 0$ and $I_i = 0$. The current through R_1 , which is the same as that through R_F , is

$$I_S = I_F = \frac{V_S}{R_1} \quad (6.68)$$

Applying Kirchhoff's voltage law around the loop formed by op-amp inputs R_F and R_2 yields

$$v_d = R_F I_F + R_2 (I_F - I_M) \quad \text{or} \quad 0 = R_F I_F + R_2 (I_F - I_M)$$

from which we can find the meter current I_M :

$$I_M = \frac{R_F + R_2}{R_2} I_F = \left(1 + \frac{R_F}{R_2}\right) I_F = \left(1 + \frac{R_F}{R_2}\right) \frac{V_S}{R_1} \quad (6.69)$$

This equation is the same as Eq. (6.64) for the optocoupler in Fig. 6.29. If $R_F \gg R_2$, which is usually the case, Eq. (6.69) can be approximated by

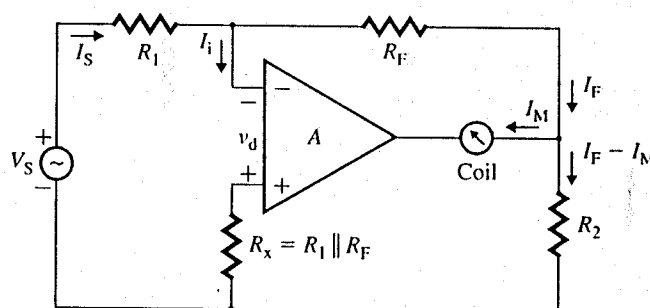
$$I_M \approx \frac{R_F}{R_1} \left(\frac{1}{R_2}\right) V_S \quad (6.70)$$

from which we can find the input voltage V_S in terms of the meter current I_M :

$$\begin{aligned} V_S &= \frac{R_1 R_2}{R_F} I_M \\ &= R_2 I_M \quad \text{for } R_1 = R_F \end{aligned} \quad (6.71)$$

If $R_1 = R_F = 150 \text{ k}\Omega$, $R_2 = 1 \text{ k}\Omega$, and the full-scale deflection current of the moving coil is $I_{M(\max)} = 100 \text{ }\mu\text{A}$, the full-scale reading will be $V_{S(\max)} = R_2 I_{M(\max)} = 1 \text{ k}\Omega \times 100 \text{ }\mu\text{A} = 100 \text{ mV}$.

FIGURE 6.33
dc millivoltmeter



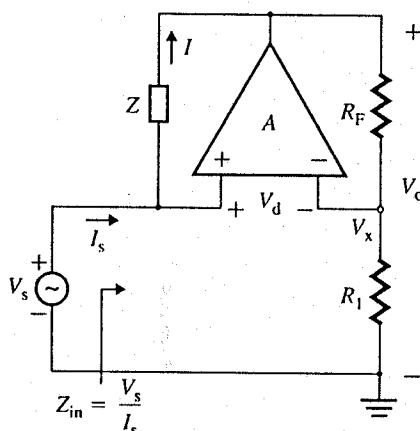
Negative Impedance Converters

Some applications (e.g., oscillators, which we will study in Chapter 11) require the characteristic of negative resistance (or impedance) in order to compensate for any undesirable resistance (or impedance). The op-amp circuit shown in Fig. 6.34 can be employed to obtain this characteristic. Since the circuit has an impedance Z , all voltages and currents will have a magnitude and a phase angle. All quantities are expressed in rms values, and we will use uppercase symbols.

Since $v_d \approx 0$,

$$V_S = V_x + v_d = V_x$$

FIGURE 6.34
Negative impedance converter



Applying Eq. (6.5) for the noninverting amplifier, we get the rms output voltage:

$$V_o = \left(1 + \frac{R_F}{R_1}\right) V_s$$

Since the current drawn by the op-amp is zero, the current I flowing through the impedance Z is the same as the input current I_s . That is,

$$I = I_s = \frac{V_s - V_o}{Z} = \frac{1}{Z} \left(V_s - V_s - \frac{R_F}{R_1} V_s \right) = -\frac{R_F}{ZR_1} V_s \quad (6.72)$$

which gives the input impedance Z_{in} as

$$Z_{in} = \frac{V_s}{I_s} = -Z \left(\frac{R_1}{R_F} \right) \quad (6.73)$$

If Z is replaced by a resistance R , then $Z = R$. The circuit will behave as a negative resistance, and Eq. (6.73) becomes

$$Z_{in} = R_{in} = -R \left(\frac{R_1}{R_F} \right) \quad (6.74)$$

Thus, the ratio R_1/R_F acts as a multiplying factor for R . If $R_1 = R_F = R$, Eq. (6.74) becomes

$$R_{in} = -R \quad (6.75)$$

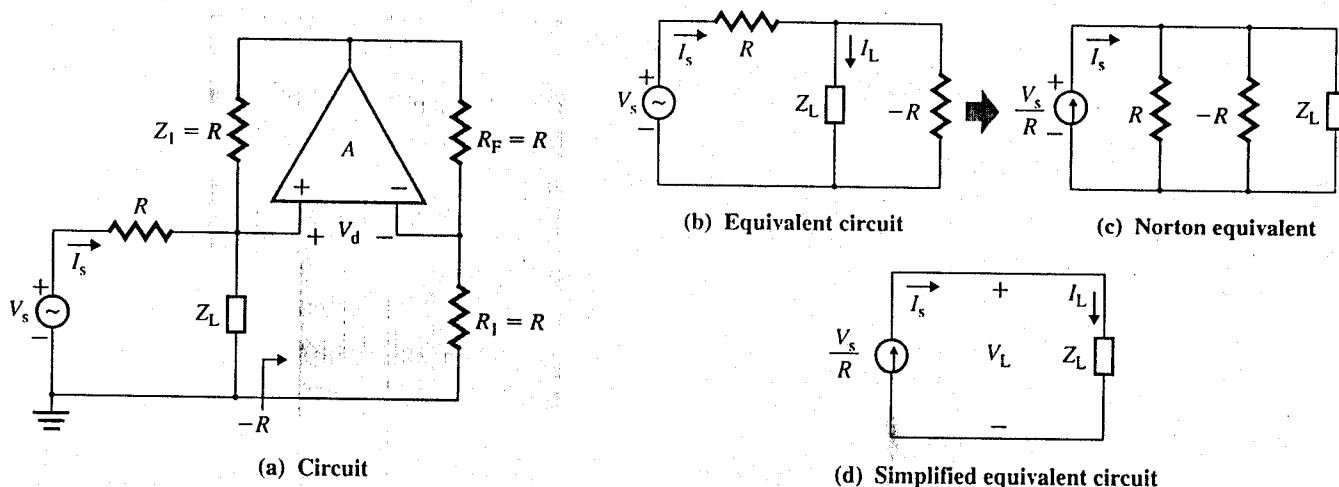
For example, if $R_1 = R_F = R = 10 \text{ k}\Omega$, the circuit in Fig. 6.34 will behave as a resistance of $R_{in} = -10 \text{ k}\Omega$.

Constant Current Sources

It is often necessary to generate a constant current source from a voltage source. The circuit of Fig. 6.34 can be modified to convert a voltage source to a current source, as shown in Fig. 6.35(a). One side of the load Z_L is connected to the ground. If $R_1 = R_F$ and $Z = R$, the input resistance becomes $R_{in} = -R$. The circuit inside the shaded area can be replaced by $-R$; the equivalent circuit is shown in Fig. 6.35(b). The voltage source V_s can be replaced by its Norton equivalent, as shown in Fig. 6.35(c). Since the parallel combination of R and $-R$ is infinite, or an open circuit, Fig. 6.35(c) can be reduced to Fig. 6.35(d). The current flowing into load impedance Z_L is simply

$$I_L = I_s = \frac{V_s}{R} \quad (6.76)$$

FIGURE 6.35 Constant current source



Noninverting Integrators

Thus, the load current I_L is directly proportional to the input voltage V_s and is independent of the load impedance Z_L . To simplify the design, one can choose $R_1 = R_F = R$.

The integrators in Figs. 6.11(a) and 6.13(a) invert the polarity of the input signal and thus require an additional unity-gain inverter to get a signal of the same polarity. The circuit of Fig. 6.35(a) can operate as a noninverting integrator if the impedance Z_L is replaced by a capacitor, as shown in Fig. 6.36(a). That is,

$$R_1 = R_F = R \quad \text{and} \quad Z_L = X_c = 1/(j\omega C)$$

Since $I_i \approx 0$, the voltage at the inverting terminal is given by

$$V_x = \frac{R_1}{R_1 + R_F} V_o = \frac{R}{R + R} V_o = \frac{V_o}{2} \quad (6.77)$$

The voltage across the capacitor is given by

$$V_c = I_L Z_L \quad (6.78)$$

For an ideal op-amp, $v_d \approx 0$. Thus,

$$V_c = V_x + v_d = V_x$$

which, after substitution of V_x from Eq. (6.77) and V_c from Eq. (6.78), gives

$$I_L Z_L = \frac{V_o}{2}$$

$$\text{or} \quad V_o = 2V_c = 2I_L Z_L \quad (6.79)$$

Substituting I_L from Eq. (6.76) into Eq. (6.79), we get

$$V_o = \frac{2Z_L V_s}{R} = \frac{2V_s}{j\omega CR} \quad (6.80)$$

which, if converted into the time domain, gives the output voltage as

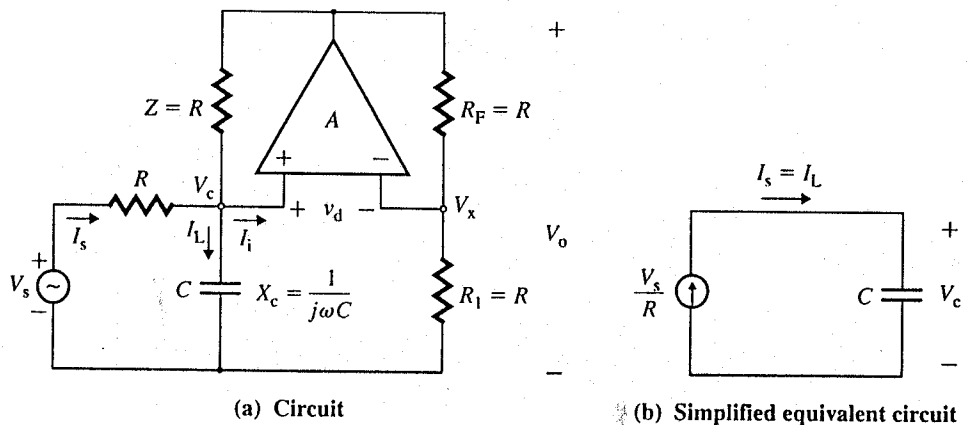
$$v_o(t) = \frac{2}{CR} \int v_s(t) dt + 2V_{co} \quad (6.81)$$

where V_{co} is the initial capacitor voltage at the beginning of integration. The charging of the capacitor can be represented by an equivalent circuit, as shown in Fig. 6.36(b). Thus, the capacitor voltage v_c can be found directly from Fig. 6.36(b) as follows:

$$v_c(t) = \frac{1}{C} \int i_s(t) dt + V_{co} = \frac{1}{RC} \int v_s dt + V_{co} \quad (6.82)$$

Thus, $v_o(t) = 2v_x(t) = 2v_c(t)$.

FIGURE 6.36
Noninverting integrator



- **NOTE:** Since one terminal of the capacitor C is grounded, the capacitor can be charged easily to a desired initial condition at the beginning of integration.

Inductance Simulators

An op-amp circuit can be used to simulate the characteristic of an inductor. Such an op-amp circuit is shown in Fig. 6.37(a). It consists of two op-amps. The part of the circuit within the shaded area is identical to the negative impedance converter of Fig. 6.34; we can apply Eq. (6.72) to replace it with an equivalent impedance provided we substitute $Z = R_3$, $R_1 = R_4$, and $R_F \equiv Z_C = 1/(j\omega C)$. Thus, the equivalent impedance is given by

$$Z_L = \frac{V_1}{I_1} = -R_3 \left(\frac{R_4}{Z_C} \right) \quad (6.83)$$

If the circuit within the shaded area is replaced by Z_L , the resultant circuit also becomes a negative impedance converter, as shown in Fig. 6.37(b). Applying Eq. (6.73) gives the input impedance of the circuit:

$$Z_{in} = \frac{V_s}{I_s} = -R_1 \left(\frac{Z_L}{R_2} \right) \quad (6.84)$$

Substituting Z_L from Eq. (6.83) into Eq. (6.84) yields

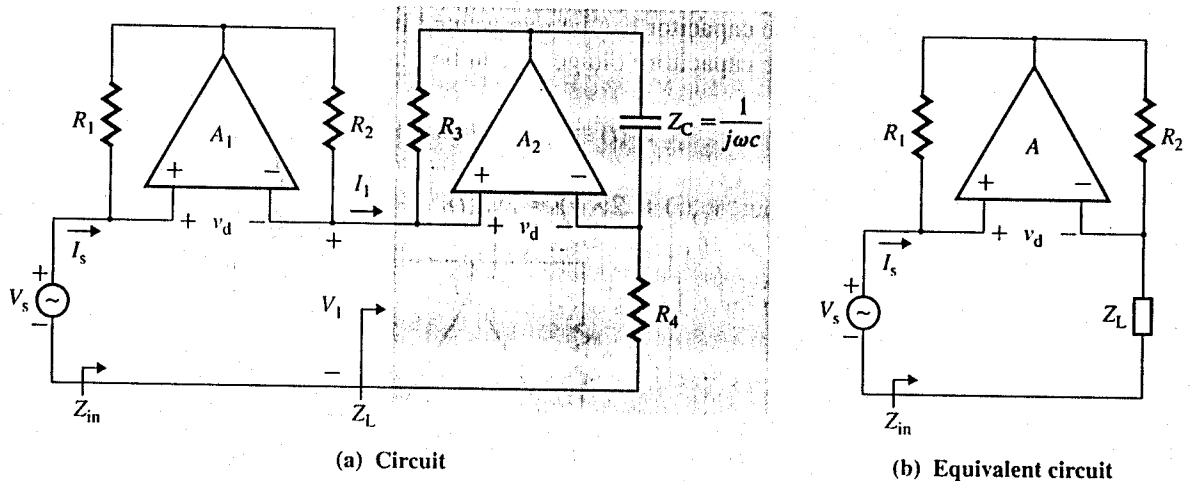
$$\begin{aligned} Z_{in} &= \frac{V_s}{I_s} = -R_1 \left(\frac{1}{R_2} \right) (-R_3) \left(\frac{R_4}{Z_C} \right) \\ &= j\omega C \frac{R_1 R_3 R_4}{R_2} = j\omega L_e \end{aligned} \quad (6.85)$$

where L_e is the effective inductance given by

$$L_e = \frac{R_1 R_3 R_4}{R_2} C \quad (6.86)$$

Therefore, by choosing the values of R_1 , R_2 , R_3 , R_4 , and C , we can simulate the desired value of inductance L_e .

FIGURE 6.37 Inductance simulator



► **NOTES:**

1. From this theoretical development it might appear that inductance simulators could be used in many applications as a replacement for bulky physical inductors. Because of the physical limitations of op-amps, however, inductance simulators suffer from many drawbacks and do not find many practical applications.

- The op-amp nonlinearities begin limiting the behavior of the inductance simulator at appallingly low frequencies (even less than 20 Hz), and the inductor does not reduce the current at high frequencies as expected.
- Inductors are commonly used in electrical power applications for storing magnetic energy. A simulated inductor cannot be used to store energy in a magnetic field, so it cannot be used in electrical power circuits (i.e., as a power filter).

EXAMPLE 6.13**D****SOLUTION**

Designing an op-amp inductance simulator Determine the values required for the components in Fig. 6.37(a) in order to simulate an inductor of $L = 1 \text{ mH}$.

Let $R_3 = R_4 = 100 \text{ k}\Omega$ and $C = 10 \text{ pF}$. From Eq. (6.86), we get

$$R_2/R_1 = R_3 R_4 C / L_e = 100 \times 10^3 \times 100 \times 10^3 \times 10 \times 10^{-12} / (1 \times 10^{-3}) = 100$$

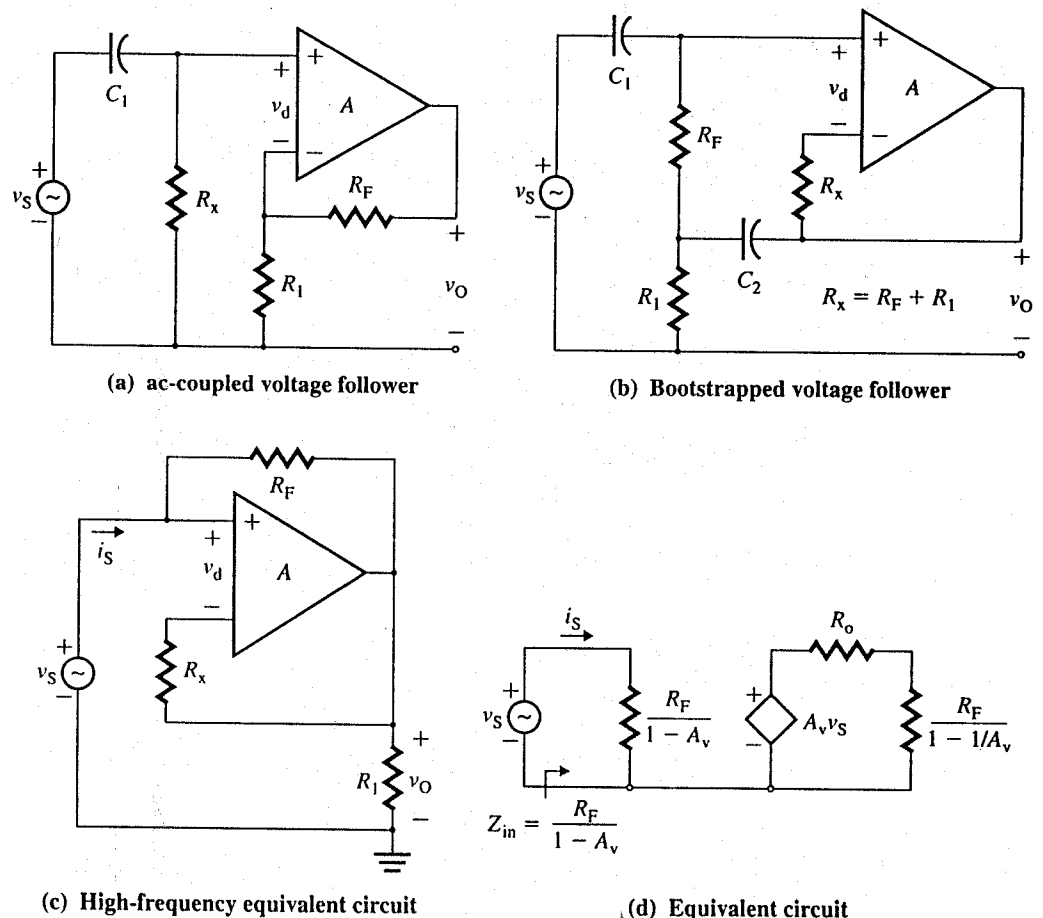
If $R_1 = 5 \text{ k}\Omega$, then $R_2 = 100 \times 5 = 500 \text{ k}\Omega$.

► **NOTE:** To use Eq. (6.86), the designer needs to know the values of five quantities in order to find the value of L_e . The designer has to assume four values, and there is no unique solution to this design problem.

ac-Coupled Bootstrapped Voltage Followers

In order to minimize the effect of dc input biasing current on the output voltage of op-amps, a resistance R_x may be connected to the noninverting terminal, as shown in Fig. 6.38(a). This reduces the effective input impedance of the voltage follower to R_x . However, the input impedance can be increased by the circuit, as shown in Fig. 6.38(b); an ac equivalent circuit is shown in Fig. 6.38(c) for higher frequencies at which the

FIGURE 6.38
ac-coupled bootstrapped
voltage follower



capacitors appear as short circuits. The op-amp is operated as a unity follower, which can be represented by an amplifier of approximately unity gain: $A_v \approx 1$. R_F appears to be connected from the input terminal to the output terminal of the amplifier, and its effect on the input impedance is the same as the Miller impedance Z_{in} connected from the input terminal to the ground. The equivalent circuit is shown in Fig. 6.38(d). From Eq. (4.95), Z_{in} is given by

$$Z_{in} = \frac{V_s}{I_s} = \frac{R_F}{1 - A_v} \quad (6.87)$$

which, for $A_v \approx 1$, yields $Z_{in} = \infty$. Since the amplifier gain is unity, the output voltage equals the input voltage and there is no voltage drop across R_F . Therefore, no current flows through R_F , and the input impedance is very high—ideally, infinity. Notice that the voltage at the end of R_F in Fig. 6.38(c) is “pulled up” to the value of the input voltage, thereby offering infinite input impedance. Because of this “bootstrap” characteristic, the circuit is known as a *bootstrapped amplifier*.

KEY POINT OF SECTION 6.5

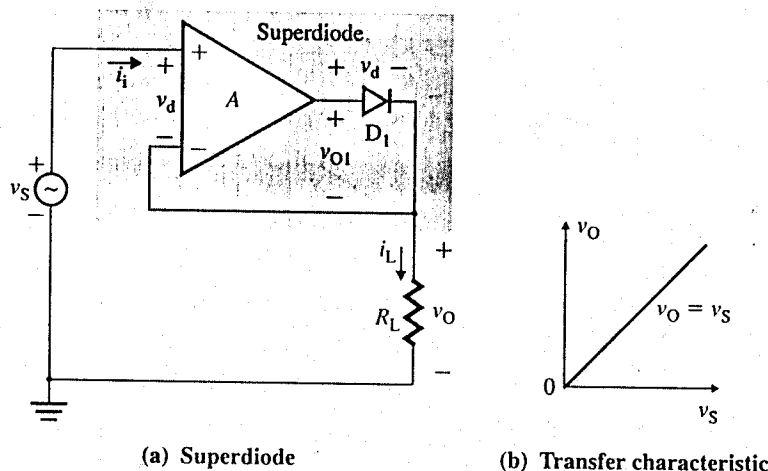
- The three basic op-amp configurations—inverting, noninverting, and differential—can be applied to perform various signal-processing functions.

6.6 Circuits with Op-Amps and Diodes

Many applications, such as peak signal detectors, precision rectifiers, comparator circuits, and limiters, require nonlinear functions. A diode, however, typically has a finite voltage drop of 0.7 V, which distorts the output voltage of a circuit with one or more diodes only, especially for low-voltage signals. Op-amp circuits with diodes can reduce the effect of diode drop and are used for precision signal processing.

Let us take the op-amp circuit shown in Fig. 6.39(a), in which the diode provides a unidirectional current flow. If the input voltage v_s is negative, the output voltage v_{O1} of the op-amp becomes negative, causing the diode to be reverse biased; no current flows through the load R_L because the current i_i flowing into the op-amp is zero. Thus, the output voltage is zero: $v_O = 0$ for $v_s \leq 0$. But the voltage v_{O1} will reach the negative saturation limit of the op-amp. If the input voltage v_s is positive, the output voltage v_{O1} of the op-amp becomes positive, causing the diode to be forward biased and supply the load current i_L .

FIGURE 6.39
Superdiode



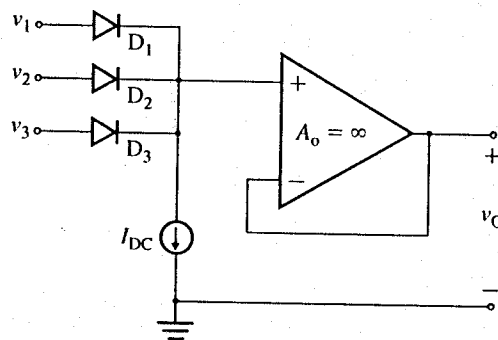
Since $v_d \approx 0$ and $i_i = 0$, the output voltage is $v_O = v_S$ for $v_S \geq 0$. The transfer characteristic of v_O versus v_S is shown in Fig. 6.39(b).

For the diode to start conduction, only a very small input voltage is required: $v_{S(\min)} = V_D/A_o$, where V_D is the diode drop (typically 0.7 V) and A_o is the open-circuit gain of the op-amp (typically 2×10^5). This circuit exhibits the characteristic of a diode. However, the effect of the diode drop is negligible. Thus, this circuit is called a *superdiode*. The drawback of this circuit is that, for negative values of v_S , the voltage v_{O1} will swing to the negative saturation limit, thereby slowing the speed of op-amp operation.

Most Positive Signal Detectors

The value of the most positive of a number of input signals can be detected by the circuit shown in Fig. 6.40. The inputs to the unity follower are the input signals to be detected. The diode that has the highest positive signal will conduct, and that signal will appear on the output of the circuit. The current source I_{DC} keeps the diode current constant irrespective of the value of the input signal, and it maintains a constant diode drop. As a result, the voltage drop across the conducting diode does not vary with variations in the input signal. Without the current source, the current and voltage of the conducting diode will change with the level of the most positive voltage, and the output voltage will vary. The unity follower acts as a buffer stage, providing a very high resistance at the diodes and a very low resistance at the output. If each diode is replaced by the superdiode shown in Fig. 6.39, there will be no voltage drop at the diodes; however, this arrangement will increase the complexity of the circuit.

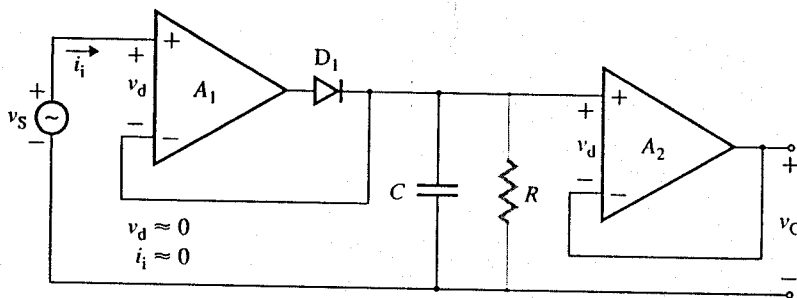
FIGURE 6.40
Positive signal detector



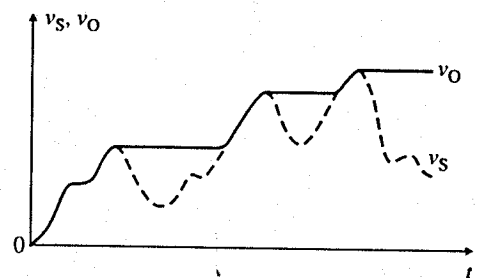
Precision Peak Voltage Detectors

A precision peak voltage detector is used in many applications, such as monitoring the peak temperature of a day (or month) or initiating the action of a device if the signal exceeds a reference value. The circuit of Fig. 6.41 will detect the peak input voltage. The superdiode circuit allows the capacitor to charge to the peak input signal. The unity follower offers a high resistance to the capacitor and supplies the capacitor voltage to the output.

FIGURE 6.41 Precision peak voltage detector



(a) Circuit diagram



(b) Waveforms for voltages

Precision Half-Wave Rectifiers

without discharging any charge of the capacitor. Resistance R , when connected, will allow the capacitor to discharge slowly so that the circuit can adjust to a lower input voltage. Otherwise, the capacitor will maintain its previous higher voltage and will not indicate the correct peak voltage.

A diode requires a minimum voltage, typically 0.7 V, to conduct. In a single-phase half-wave rectifier, one diode conducts. If the input voltage is less than 0.7 V, the output of the rectifier will be zero. Therefore, diode rectifiers are not suitable for rectification of low voltage. An op-amp circuit with two diodes, as shown in Fig. 6.42(a), can rectify a very small voltage in the range of μV . The circuit operation can be divided into two intervals: interval 1 and interval 2. We will consider the circuit operation with a sinusoidal input voltage $v_S = V_m \sin \omega t$.

During interval 1, $0 \leq \omega t \leq \pi$. The input voltage is positive. The voltage v_{O1} at the output of the first op-amp is negative, and diode D_2 is off. Diode D_1 conducts, and current i_f through R_3 equals input current i_S . Since the current flowing into the op-amp is zero, $i_S = i_f$ and

$$i_S = i_f = \frac{v_S}{R_1}$$

$$v_d = R_F i_f + v_{O2}$$

For an ideal op-amp, $v_d = 0$, and voltage v_{O2} becomes

$$v_{O2} = -R_F i_f = -R_1 i_f = -R_1 i_S \quad (\text{for } R_F = R_1)$$

$$= -v_S \quad (\text{for } R_3 = R_2 = R_1 \text{ and for } v_S \geq 0)$$

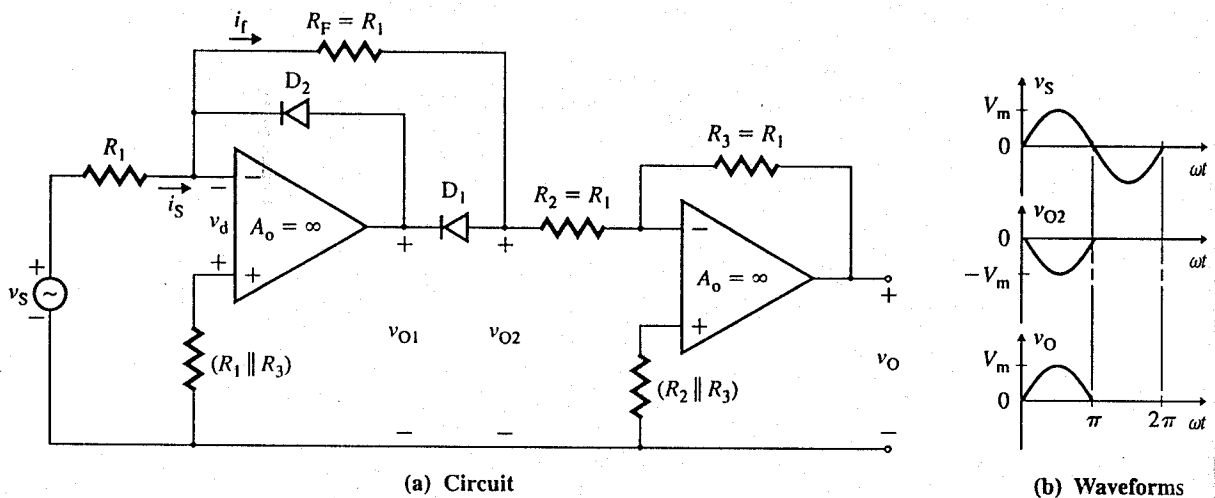
Thus, the output voltage at the output of the second inverting op-amp is

$$v_O = -v_{O2} = v_S \quad \text{for } v_S \geq 0$$

During interval 2, $\pi \leq \omega t \leq 2\pi$. The input voltage is negative. The voltage v_{O1} at the output of the first op-amp is positive, and diode D_2 conducts. As a result, the voltage v_{O1} is clamped to approximately the voltage of one diode. Diode D_1 remains off, and no current flows through R_F . The voltage v_{O2} becomes zero. Thus, the output voltage at the output of the second op-amp is $v_O = -v_{O2} = 0$.

The output voltage v_O is almost independent of the diode characteristics. This is because diode D_1 is included in series with the op-amp. Since the op-amp gain is very high,

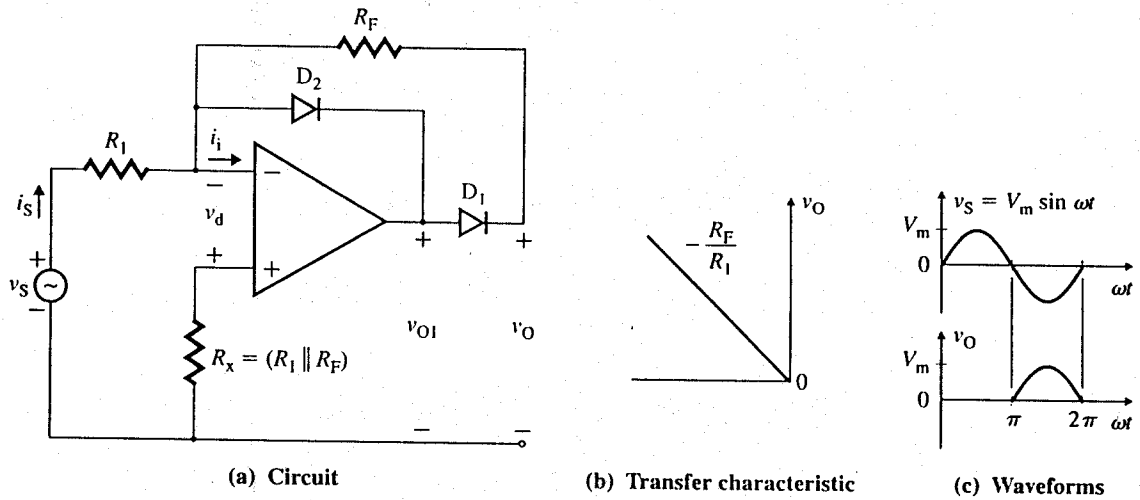
FIGURE 6.42 Precision half-wave rectifier



tending to infinity, the effect of the diode and its voltage drop becomes insignificant. The output waveforms are shown in Fig. 6.42(b).

If the directions of the diodes are reversed, the output voltage will correspond to the negative part of the input voltage; there is no need for the second inverting op-amp. This arrangement is shown in Fig. 6.43(a). When the input voltage v_S is positive, the voltage v_{O1} becomes negative, making diode D_2 conduct and diode D_1 turn off. As a result, the output voltage becomes zero. That is, the output voltage $v_O = 0$ for $v_S \geq 0$. On the other hand, when the input voltage v_S is negative, the voltage v_{O1} becomes positive, making diode D_2 turn off and diode D_1 conduct. As a result, the output voltage will be equal and opposite to the input voltage. That is, the output voltage $v_O = -v_S$ for $v_S < 0$. The transfer characteristic is shown in Fig. 6.43(b), and the voltage waveforms are shown in Fig. 6.43(c).

FIGURE 6.43 Alternate precision half-wave rectifier



Precision Full-Wave Rectifiers

The half-wave rectifier of Fig. 6.43(a) can be modified to operate as a precision full-wave rectifier if we use the following algebraic relationship:

$$v_O = 2v_S - v_{O2} = v_S \quad \text{for the positive interval of the input voltage}$$

This situation is shown in Fig. 6.44(a). Let us consider the case with $R_1 = R_2 = R_F = R$ and $R_3 = R_4 = 2R$. We will divide the circuit operation into two intervals, interval 1 and interval 2, and use a sinusoidal input voltage $v_S = V_m \sin \omega t$.

During interval 1, $0 \leq \omega t \leq \pi$, v_S is positive, and $v_{O2} = -v_S$. The voltage at the output of the second op-amp can be found from

$$v_O = -\left(\frac{R_3}{R_2} v_{O2} + \frac{R_3}{R_4} v_S\right) \quad (6.88)$$

which, for $R_3 = R_4 = 2R$ and $R_2 = R$, becomes

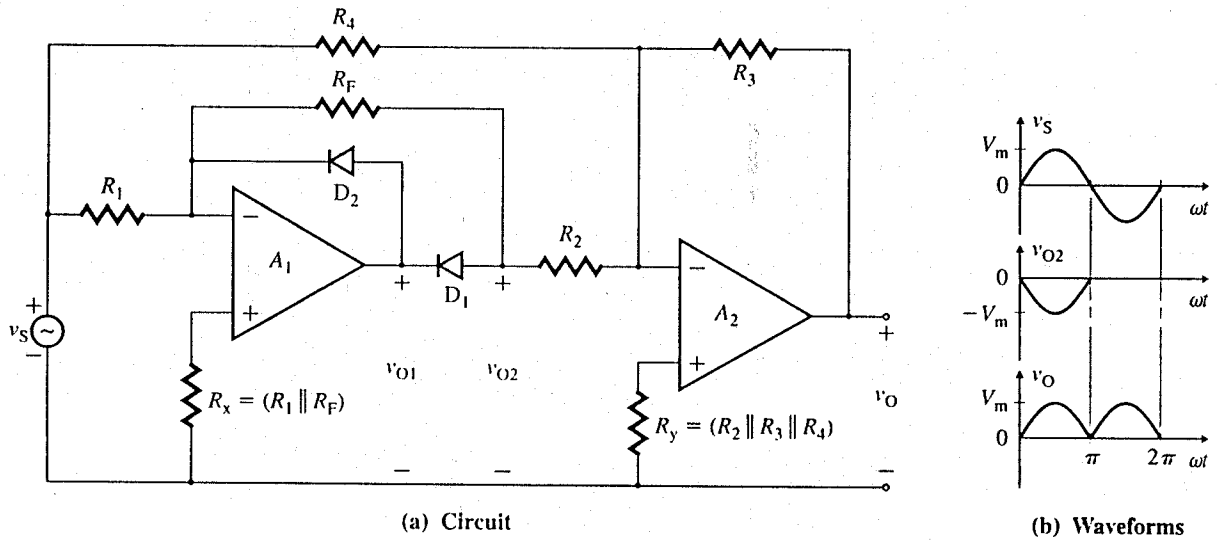
$$v_O = -2v_{O2} - v_S = -2(-v_S) - v_S = v_S \quad \text{for } v_S \geq 0$$

During interval 2, $\pi \leq \omega t \leq 2\pi$, v_S is negative, and $v_{O2} = 0$. The voltage at the output of the second op-amp can be found from

$$v_O = -\left(\frac{R_3}{R_2} v_{O2} + \frac{R_3}{R_4} v_S\right) \quad (6.89)$$

which, for $R_3 = R_4 = 2R$ and $R_2 = R$, becomes

$$v_O = -2v_{O2} - v_S = -2 \times 0 - v_S = -v_S \quad \text{for } v_S < 0$$

FIGURE 6.44 Precision full-wave rectifier

Thus, the output voltage is the inverted version of the input voltage, as shown in Fig. 6.44(b).

Precision Clamping Circuits

A precision clamping circuit is sometimes used in signal processing in order to add just enough dc voltage to the input voltage so that the sum never crosses the zero level. Figure 6.45(a) shows a superdiode circuit with an input voltage v_S and a dc reference voltage V_{ref} . As long as the op-amp voltage v_d is positive, v_{O1} will be positive and diode D_1 will conduct, thereby making the $(-)$ terminal behave as a virtual ground. To consider the circuit operation, let us take a sinusoidal input voltage $v_S = V_m \sin \omega t$ and $V_{ref} = 0$.

During the interval $0 \leq \omega t \leq \pi$, v_S is positive, v_d is negative, v_{O1} is negative, and diode D_1 is reverse biased. No current flows through the capacitor, and it cannot charge. During the interval $\pi < \omega t \leq 3\pi/2$, v_S is negative, v_d is positive, v_{O1} is positive, and diode D_1 conducts. The $(-)$ terminal behaves as a virtual ground. A charging current flows through the capacitor, with point A being at a higher potential than point B. The capacitor is charged to the peak negative voltage V_m . For the interval $\omega t > 3\pi/2$,

$$v_d = -(V_m + v_S) = -V_m(1 + \sin \omega t)$$

and diode D_1 remains off. That is, the output voltage v_O is

$$v_O = -v_d = V_m(1 + \sin \omega t)$$

The voltage waveforms are shown in Fig. 6.45(b). With a reference voltage of V_{ref} , the capacitor will charge to $(V_m + V_{ref})$, and the output voltage v_O can be expressed by

$$v_O = V_m \sin \omega t + V_m + V_{ref} \quad (6.90)$$

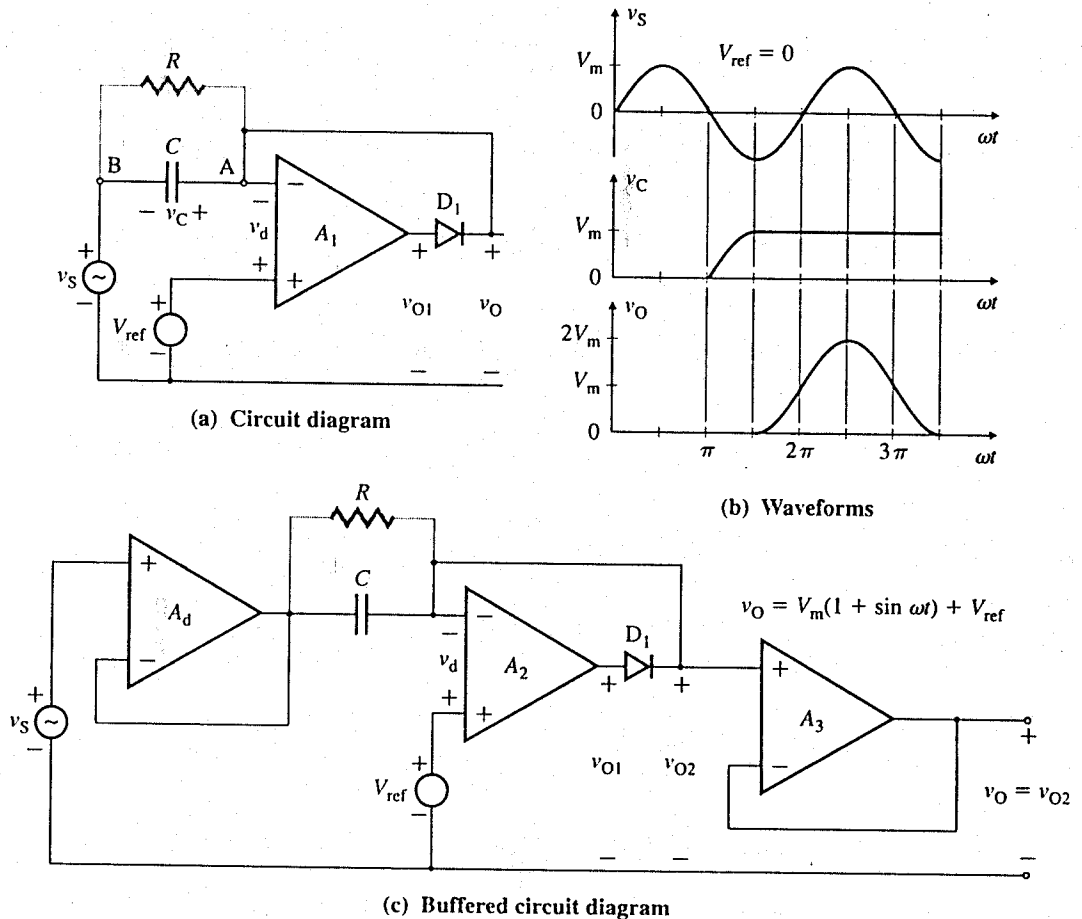
For example, for $V_m = 10$ V and $V_{ref} = 5$ V, $v_O = 10 \sin \omega t + 15$ V, and for $V_m = 10$ V and $V_{ref} = -5$ V, $v_O = 10 \sin \omega t + 5$ V. If the direction of diode D_1 is reversed, the capacitor will charge when v_d becomes negative during the interval $0 \leq \omega t \leq \pi/2$. The output voltage will then be reversed. That is,

$$v_O = -(V_m \sin \omega t + V_m + V_{ref})$$

A resistor R , represented in Fig. 6.45(a) by a light line, can be connected across the capacitor so that the capacitor can discharge slowly and the circuit can adjust to an input voltage of lower amplitude. The resistor can also provide a path for the dc biasing current

FIGURE 6.45

Precision clamping circuit



of the op-amp. As shown in Fig. 6.45(c), voltage followers may be connected to the input and output sides so that the clamping circuit draws no current from the signal source and can deliver load current without affecting the charge on the capacitor.

Fixed-Voltage Limiters

A limiter restricts the output voltage to a specified value. A negative output voltage can be limited approximately to zero by connecting a diode across the feedback resistor R_F of the inverting amplifier in Fig. 6.9, as shown in Fig. 6.46(a). If the input voltage v_S is positive, the output voltage v_O tends to be negative, and diode D_1 conducts, limiting the output to a negative value $-V_D$ of the diode voltage drop. If the input voltage is negative, the output

FIGURE 6.46

Negative voltage limiter

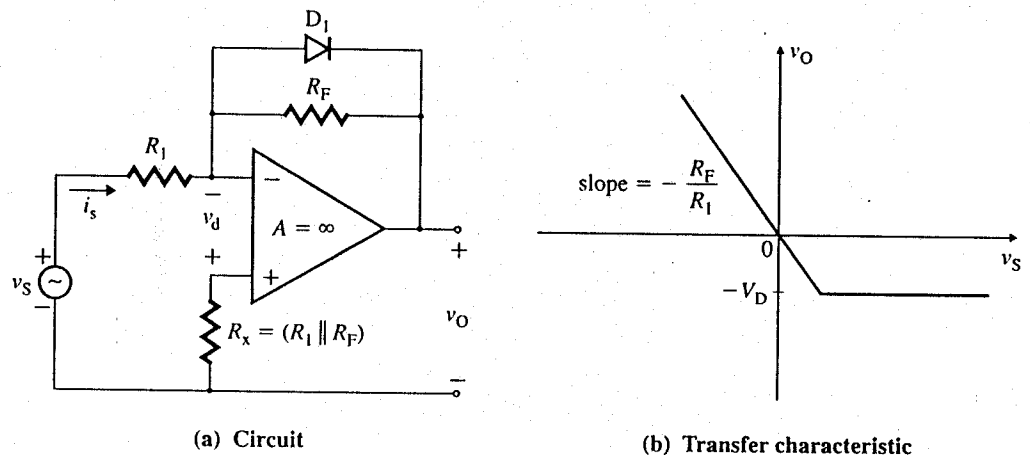
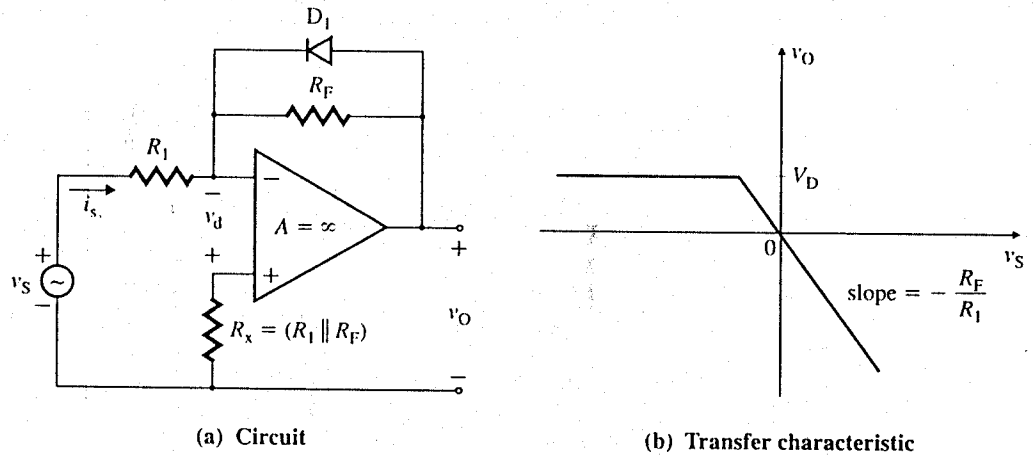


FIGURE 6.47
Positive voltage limiter

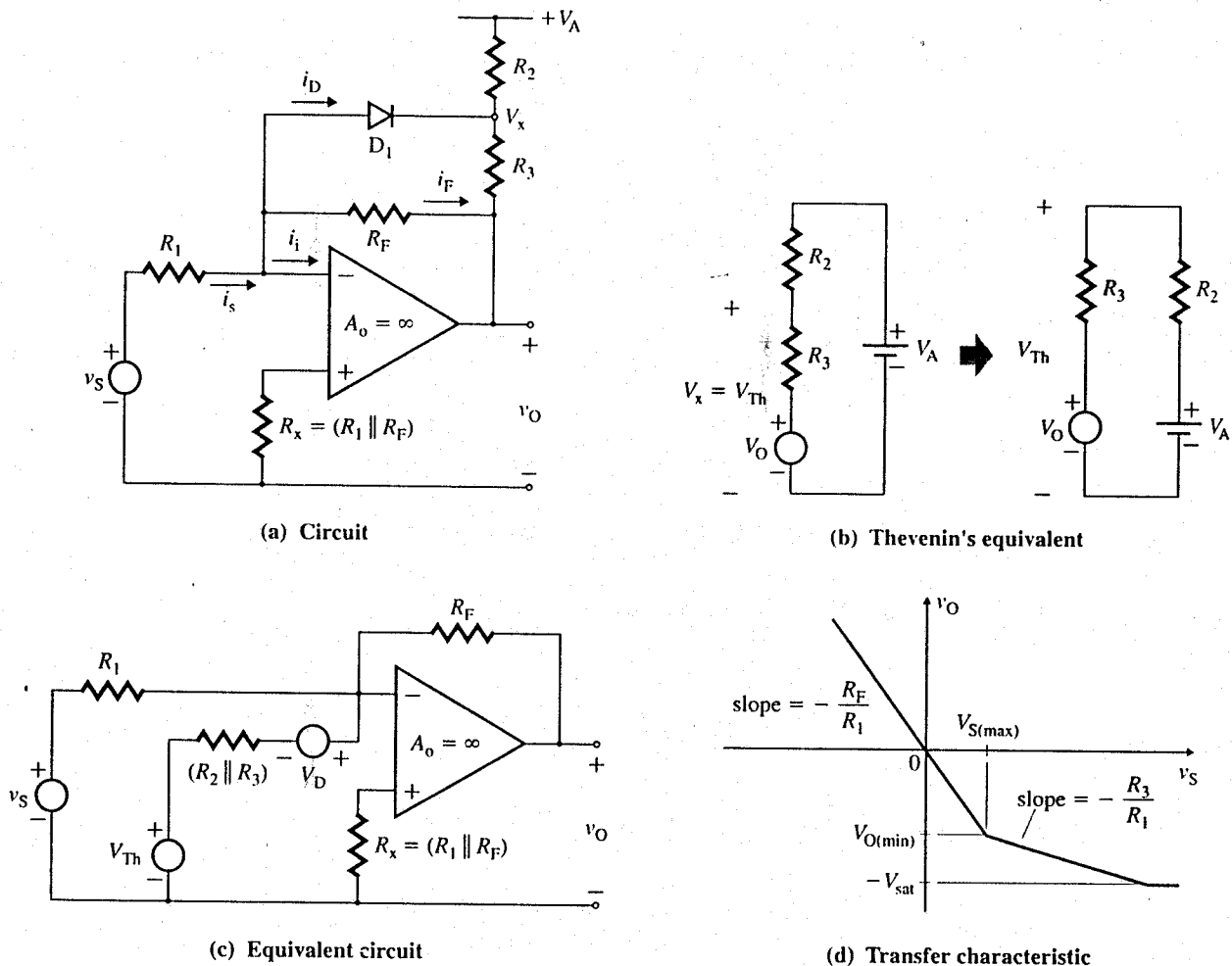


voltage becomes positive, and the diode is reverse biased. The output voltage follows the input voltage with a change in polarity. The transfer characteristic is shown in Fig. 6.46(b). If the direction of the diode is reversed, as shown in Fig. 6.47(a), the positive output voltage is limited to V_D , as shown by the transfer characteristic in Fig. 6.47(b).

Adjustable Voltage Limiters

Output voltage can be limited to an adjustable level by choosing resistors with appropriate values. A circuit that limits the negative output voltage is shown in Fig. 6.48(a). If the output is positive, diode D_1 is reverse biased, and the circuit operates as an inverting

FIGURE 6.48 Adjustable negative voltage limiter



amplifier. If the output voltage is negative, its transfer characteristic changes its slope at $v_{O(\min)}$ and then varies with a slope of $-R_3/R_1$. The circuit operation can be divided into two intervals: interval 1 and interval 2.

During interval 1, diode D_1 is reverse biased and remains off. The circuit operates as an inverting amplifier, and the slope of the transfer characteristic is $-R_F/R_1$.

During interval 2, diode D_1 conducts, and the limiting circuit is active. Let V_D be the forward diode drop. D_1 is turned on when the potential V_x becomes $-V_D$. Voltage V_x can be found from Thevenin's equivalent circuit, as shown in Fig. 6.48(b). By the superposition theorem (considering sources v_O and V_A separately), Thevenin's equivalent voltage is given by

$$V_{Th} = \frac{R_2 v_O}{R_2 + R_3} + \frac{R_3 V_A}{R_2 + R_3}$$

Diode D_1 turns on when $V_x = -V_D$. That is,

$$V_x = -V_D = V_{Th} = \frac{R_2 v_O}{R_2 + R_3} + \frac{R_3 V_A}{R_2 + R_3} \quad (6.91)$$

which gives the negative clamping output voltage $V_{O(\min)}$ as

$$V_{O(\min)} = v_O = -V_D - (V_A + V_D) \frac{R_3}{R_2} = -V_D \left(1 + \frac{R_3}{R_2}\right) - V_A \frac{R_3}{R_2} \quad (6.92)$$

from which the positive input voltage corresponding to $V_{O(\min)}$ can be found:

$$V_{S(\max)} = -\frac{R_1}{R_F} v_{O(\min)} = \frac{R_1}{R_F} \left[\frac{R_3}{R_2} V_A + \left(1 + \frac{R_3}{R_2}\right) V_D \right] \quad (6.93)$$

$(V_{Th} - V_D)$ acts a reference voltage V_{ref} . Then v_S can be compared to V_{ref} . $V_{S(\max)}$ is the threshold voltage at which the change of slope takes place. The equivalent circuit in Fig. 6.48(c) has two input signals, v_S and $(V_{Th} - V_D)$, and it can be characterized as a summing amplifier. The output voltage during the clamped condition can be expressed as

$$v_O = -\frac{R_F v_S}{R_1} - \frac{R_F}{(R_2 \parallel R_3)} \left(\frac{R_2 v_O}{R_2 + R_3} + \frac{R_3 V_A}{R_2 + R_3} + V_D \right)$$

which, after solving for v_O , gives

$$v_O = -\frac{1}{1 + R_F/R_3} \left[\frac{R_F}{R_1} v_S + \frac{R_F}{R_2} V_A + \frac{R_F}{(R_2 \parallel R_3)} V_D \right] \quad (6.94)$$

For $R_F/R_3 \gg 1$, which is normally the case, Eq. (6.94) is reduced to

$$v_O = -\frac{R_3}{R_1} v_S - \frac{R_3}{R_2} V_A - \left(1 + \frac{R_3}{R_2}\right) V_D \quad \text{for } v_S > 0 \quad (6.95)$$

which describes the transfer characteristic of the limiter, as shown in Fig. 6.48(d). The slope beyond the break point is $-R_3/R_1$, and this slope should be made small by choosing $R_1 \gg R_3$. Note that $|V_{O(\min)}|$ must be less than the saturation voltage $|V_{sat}|$ of the op-amp.

The positive voltage can be limited by adding another diode D_2 , as shown in Fig. 6.49(a). V_x and V_y limit the negative voltage and positive voltage, respectively. V_y can be found from Eq. (6.91):

$$V_y = V_D = V_{Th1} = \frac{R_4 v_O}{R_4 + R_5} + \frac{R_5 V_B}{R_4 + R_5} \quad (6.96)$$

Similarly, the positive clamping voltage can be found from Eq. (6.92):

$$V_{O(\max)} = v_O = V_D + (V_B + V_D) \frac{R_5}{R_4} = V_D \left(1 + \frac{R_5}{R_4}\right) + V_B \frac{R_5}{R_4} \quad (6.97)$$

The negative input voltage corresponding to $V_{O(\max)}$ can be found from

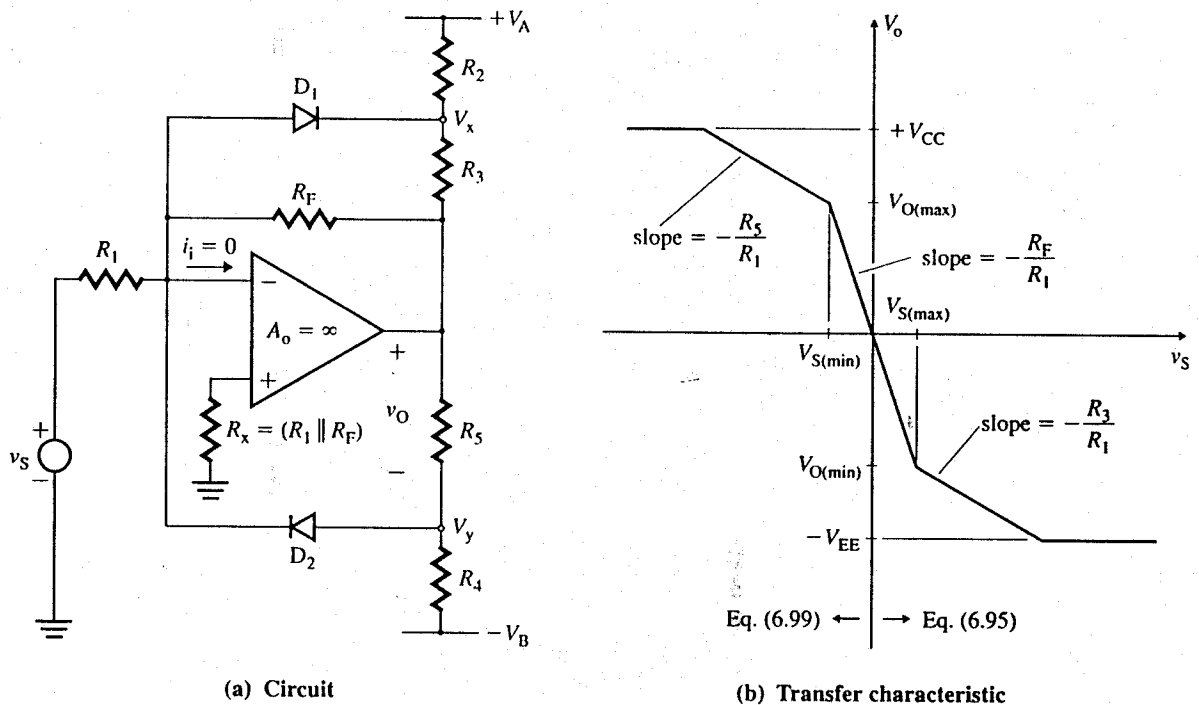
$$V_{S(\min)} = -\frac{R_1}{R_F} V_{O(\max)} = -\frac{R_1}{R_F} \left[\frac{R_5}{R_4} V_B + \left(1 + \frac{R_5}{R_4}\right) V_D \right] \quad (6.98)$$

$(V_{Th1} - V_D)$ acts a reference voltage V_{ref1} . Then v_S can be compared to V_{ref1} . $V_{S(\min)}$ is the threshold voltage at which the change of slope takes place. Using Eq. (6.94), we can find the output voltage during the positive voltage clamping to be

$$v_O = \frac{R_5}{R_1} v_S + \frac{R_5}{R_4} V_B + \left(1 + \frac{R_5}{R_4}\right) V_D \quad \text{for } v_S < 0 \quad (6.99)$$

which describes the transfer characteristic of an adjustable positive and negative voltage limiter, as shown in Fig. 6.49(b). This is a practical limiter and is commonly used. It is also called a *soft limiter*, since the output voltage will increase slightly if the input voltage is increased beyond the break points. All dc supply voltages of the limiter are generally made the same magnitude. That is, $V_A = V_B = V_{CC} = V_{EE}$.

FIGURE 6.49 Adjustable positive and negative voltage limiter



EXAMPLE 6.14

D

Designing a negative voltage limiting circuit Design a negative voltage limiter as shown in Fig. 6.48(a) for $V_A = 12$ V. The circuit should limit the negative output voltage to $V_{O(\min)} = -5$ V. The voltage gain without limiting is $A_f = -4$. The diode should be fully turned on at a forward current of $i_D = 0.1$ mA, and its forward voltage drop is $V_D = 0.7$ V. The slope after the break point is to be limited to $-1/20$. Determine the values of R_1 , R_2 , R_3 , and R_F .

SOLUTION

Equation (6.93) gives the diode current at clamping as

$$i_D = \frac{V_{S(\max)}}{R_1} = -\frac{1}{R_F} V_{O(\min)}$$

so $0.1 \times 10^{-3} = -(-5)/R_F$

or $R_F = 50 \text{ k}\Omega$

Since $A_f = -4 = -R_F/R_1$,

$$R_1 = R_F/4 = 50 \text{ k}/4 = 12.5 \text{ k}\Omega$$

Since slope $S = -R_3/R_1 = -1/20$,

$$R_3 = R_1/20 = 12.5 \text{ k}/20 = 625 \Omega$$

From Eq. (6.92),

$$-5 = -0.7 - (12 + 0.7) R_3/R_2$$

$$R_3/R_2 = 0.3386$$

$$R_2 = R_3/0.3386 = 625/0.3386 = 1846 \Omega$$

EXAMPLE 6.15

Finding the limiting voltages of an op-amp limiting circuit The adjustable limiter in Fig. 6.49(a) has $R_1 = 15 \text{ k}\Omega$, $R_F = 60 \text{ k}\Omega$, $R_2 = 4 \text{ k}\Omega$, $R_3 = 1 \text{ k}\Omega$, $R_4 = 5 \text{ k}\Omega$, $R_5 = 1 \text{ k}\Omega$, $V_A = 15 \text{ V}$, $-V_B = -15 \text{ V}$, and $V_D = 0.7 \text{ V}$. Determine (a) the positive clamping voltage $V_{O(\max)}$ and the corresponding input voltage $V_{S(\min)}$, (b) the negative clamping voltage $V_{O(\min)}$ and the corresponding input voltage $V_{S(\max)}$, and (c) the output voltage when the input voltage is $v_S = 5 \text{ V}$.

SOLUTION

$R_1 = 15 \text{ k}\Omega$, $R_F = 60 \text{ k}\Omega$, $R_2 = 4 \text{ k}\Omega$, $R_3 = 1 \text{ k}\Omega$, $R_4 = 5 \text{ k}\Omega$, $R_5 = 1 \text{ k}\Omega$, $V_A = 15 \text{ V}$, $-V_B = -15 \text{ V}$, $V_D = 0.7 \text{ V}$, and $v_S = 5 \text{ V}$.

(a) From Eq. (6.97),

$$V_{O(\max)} = 0.7 + (15 + 0.7) \times 1 \text{ k}/5 \text{ k} = 3.84 \text{ V}$$

From Eq. (6.98),

$$V_{S(\min)} = -V_{O(\max)} R_1/R_F = -3.84 \times 15 \text{ k}/60 \text{ k} = -0.96 \text{ V}$$

(b) From Eq. (6.92),

$$V_{O(\min)} = -0.7 - (15 + 0.7) \times 1 \text{ k}/4 \text{ k} = -4.625 \text{ V}$$

From Eq. (6.93),

$$V_{S(\max)} = -V_{O(\min)} R_1/R_F = 4.625 \times 15 \text{ k}/60 \text{ k} = 1.15625 \text{ V}$$

(c) From Eq. (6.95),

$$v_O = -5 \times 1 \text{ k}/15 \text{ k} - 15 \times 1 \text{ k}/4 \text{ k} - (1 + 1 \text{ k}/4 \text{ k}) \times 0.7 = -4.958 \text{ V}$$

EXAMPLE 6.16

D

Designing an adjustable voltage limiting circuit

(a) Design an adjustable limiter as shown in Fig. 6.49(a) to satisfy the following specifications: $V_A = 12 \text{ V}$, $-V_B = -12 \text{ V}$, $V_{O(\min)} = -5 \text{ V}$, $V_{O(\max)} = 6 \text{ V}$, voltage gain $A_f = -4$, slope after break with a positive input (for $v_S > 0$) = $S_1 = -1/20$, and slope after break with a negative input (for $v_S < 0$) = $S_2 = -1/25$. Assume that the diode is fully on at a diode current of $i_D = 0.1 \text{ mA}$ and the corresponding on-state diode voltage is $V_D = 0.7 \text{ V}$.

(b) Use PSpice/SPICE to plot the transfer characteristic v_O versus $v_S = V(6)$. Assume $V_{CC} = 12 \text{ V}$ and $-V_{EE} = -12 \text{ V}$.

SOLUTION

(a) The steps in completing the design are as follows.

Step 1. The diode current can be related to $V_{O(\min)}$ and R_F by

$$i_D = -\frac{V_{O(\min)}}{R_F} \quad \text{or} \quad 0.1 \text{ mA} = -\frac{-5}{R_F}$$

which gives $R_F = 50 \text{ k}\Omega$.

Step 2. The voltage gain A_f is given by

$$A_f = -\frac{R_F}{R_1} \quad \text{or} \quad -4 = -\frac{50 \text{ k}\Omega}{R_1}$$

which gives $R_1 = 12.5 \text{ k}\Omega$.

Step 3. The slope after break with a positive input (for $v_S > 0$) is

$$S_1 = -\frac{R_3}{R_1} \quad \text{or} \quad -\frac{1}{20} = -\frac{R_3}{12.5 \text{ k}\Omega}$$

which gives $R_3 = 625 \Omega$.

Step 4. The slope after break with a negative input (for $v_S < 0$) is

$$S_2 = -\frac{R_5}{R_1} \quad \text{or} \quad -\frac{1}{25} = -\frac{R_5}{12.5 \text{ k}\Omega}$$

which gives $R_5 = 500 \Omega$.

Step 5. The value of R_2 can be found from Eq. (6.92):

$$V_{O(\min)} = -V_D - (V_A + V_D) \frac{R_3}{R_2} \quad \text{or} \quad -5 = -0.7 - (12 + 0.7) \frac{625}{R_2}$$

which gives $R_2 = 1846 \Omega$.

Step 6. The value of R_4 can be found from Eq. (6.97):

$$V_{O(\max)} = V_D + (V_B + V_D) \frac{R_5}{R_4} \quad \text{or} \quad 6 = 0.7 + (12 + 0.7) \frac{500}{R_4}$$

which gives $R_4 = 1198 \Omega$.

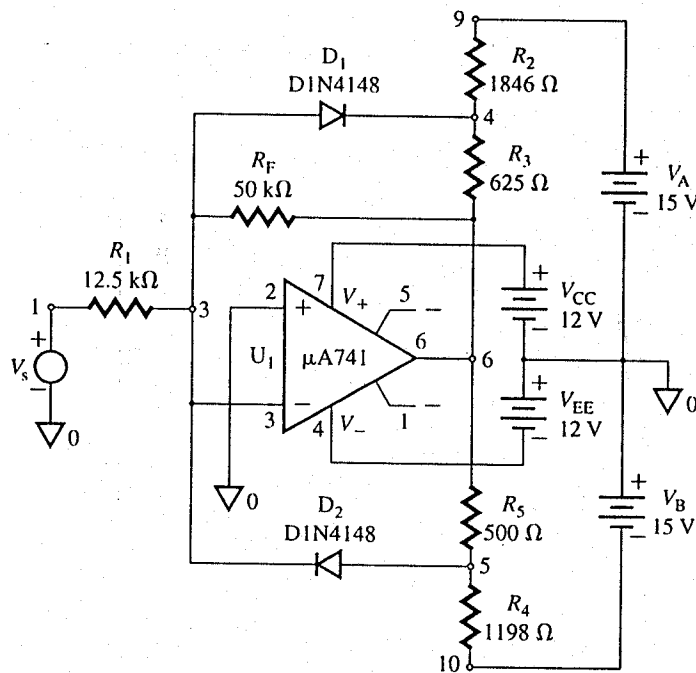
(b) The limiter circuit for PSpice simulation is shown in Fig. 6.50. The list of the circuit file is as follows.

Example 6.16 Voltage Limiter

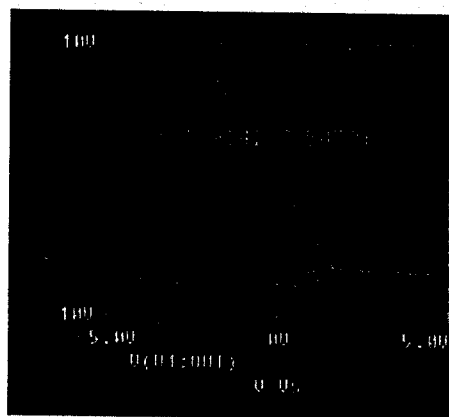
```

Vs 1 0 DC 6V
VCC 7 0 DC 12V
VEE 0 8 DC 12V
VA 9 0 DC 12V
VB 0 10 DC 12V
RF 3 6 50K
R1 1 3 12.5K
R2 4 9 1846
R3 4 6 625
R5 5 6 500
R4 5 10 1198
RX 2 0 10K
D1 3 4 DMOD           ; Diode with model DMOD
D2 5 3 DMOD
.MODEL DMOD D          ; Diode model with default parameters
.LIB NOM.LIB            ; Referring to PSpice library file NOM.LIB for
                        ; UA741 op-amp model
XA1 2 3 7 8 6 UA741    ; Subcircuit call for op-amp UA741
* vi+ vi- +vcc -vee vo
.DC Vs -6V 6V 0.05V    ; dc sweep for -6 V to 6 V
.PROBE                  ; Graphics post-processor
.END

```

FIGURE 6.50 Limiter circuit for PSpice simulation

The transfer characteristic (for EX6-16.SCH) is shown in Fig. 6.51, which gives $V_{S(\max)} = 1.67\text{ V}$, $V_{S(\min)} = -1.91\text{ V}$, $V_{O(\max)} = 7.5\text{ V}$ (expected value is 6 V), and $V_{O(\min)} = -6.4\text{ V}$ (expected value is -5 V). The discrepancies between the design values and the PSpice results may be attributed to the use of an ideal op-amp versus a macromodel and the use of a specific diode versus a diode of type D1N4148. If we run the simulation using EX6-16.CIR, the PSpice and calculated values will agree more closely.

FIGURE 6.51 PSpice transfer characteristic for Example 6.16

Zener Voltage Limiters

The output can be limited by adding two zener diodes across the output terminals of a non-inverting or an inverting amplifier. An arrangement for a noninverting amplifier circuit is shown in Fig. 6.52(a). Zener diodes limit the output voltage between $-(V_{Z2} + V_D)$ and $(V_{Z1} + V_D)$, where V_D is the voltage drop of a zener diode in the forward direction. Without

zener action, the output voltage can be found by using Eq. (6.5) for the noninverting amplifier:

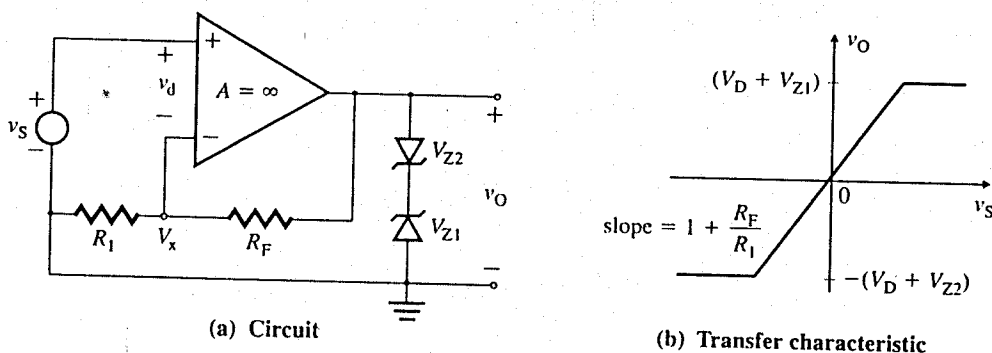
$$v_O = \left(1 + \frac{R_F}{R_I}\right) v_S$$

If the output voltage is to be limited to a maximum voltage $V_{O(\max)} = v_O = (V_{Z1} + V_D)$ and a minimum voltage $V_{O(\min)} = v_O = -(V_{Z2} + V_D)$, it can be expressed as

$$v_O = \begin{cases} V_{Z1} + V_D = V_{O(\max)} & \text{for } v_O > V_{O(\max)} \\ -(V_{Z2} + V_D) = V_{O(\min)} & \text{for } v_O < V_{O(\min)} \\ \left(1 + \frac{R_F}{R_I}\right) v_S & \text{for } V_{O(\min)} \leq v_O \leq V_{O(\max)} \end{cases}$$

The transfer characteristic is shown in Fig. 6.52(b).

FIGURE 6.52
Output voltage clamp
circuit with zener diodes



EXAMPLE 6.17

D

SOLUTION

Designing a zener voltage clamping circuit Design an output voltage clamping circuit as shown in Fig. 6.52(a) so that the normal slope of the transfer characteristic is $S = v_O/v_S = 10$, $V_{O(\max)} = 5.7$ V, and $V_{O(\min)} = -7.7$ V. Determine the zener voltages V_{Z1} and V_{Z2} . Assume $V_D = 0.7$ V.

$V_{O(\max)} = 5.7$ V, and $V_{O(\min)} = -7.7$ V. Since $S = 1 + R_F/R_I = 10$,

$$R_F/R_I = 10 - 1 = 9$$

If $R_I = 5$ k Ω ,

$$R_F = 9 \times 5 \text{ k} = 45 \text{ k}\Omega$$

Since $V_{O(\max)} = (V_{Z1} + V_D)$,

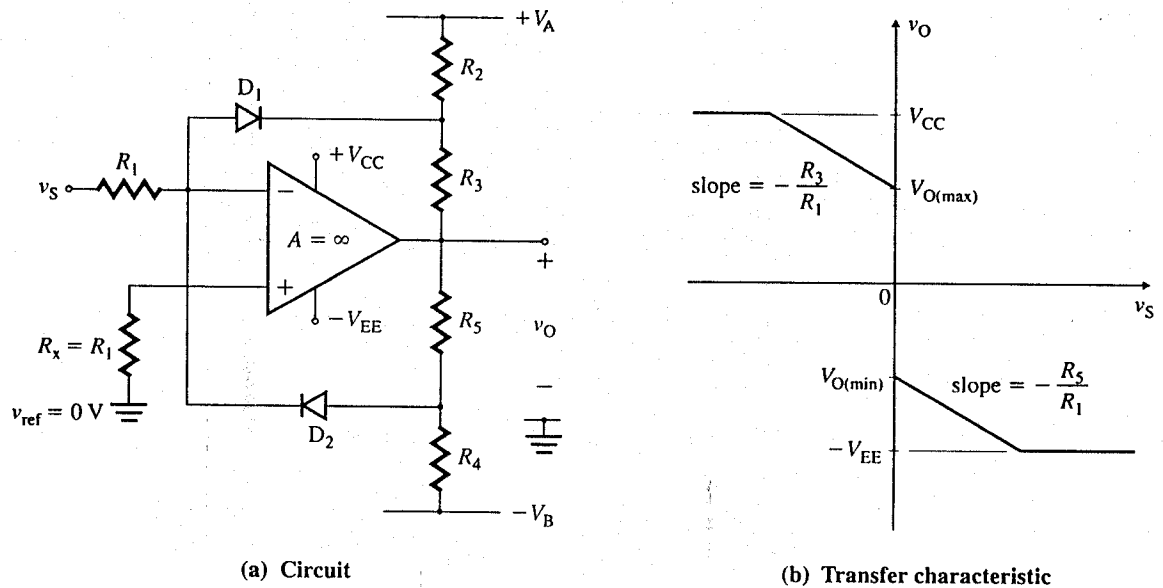
$$V_{Z1} = V_{O(\max)} - V_D = 5.7 - 0.7 = 5 \text{ V}$$

Since $V_{O(\min)} = -(V_{Z2} + V_D)$,

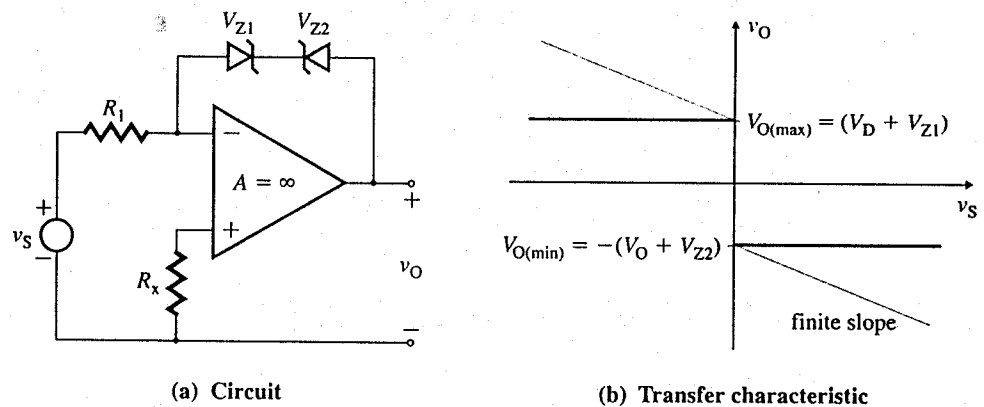
$$V_{Z2} = -(V_{O(\min)} + V_D) = -(-7.7 + 0.7) = 7 \text{ V}$$

Hard Limiters

The limiter in Fig. 6.49(a) can be made to switch between $V_{O(\min)}$ and $V_{O(\max)}$ if the input voltage v_S becomes greater than zero or less than zero, respectively. This can be accomplished by making the feedback resistance R_F in Fig. 6.49(a) very large, tending to infinity. That is, for $R_F = \infty$, the gain of the circuit becomes very large, tending to infinity, and the output voltage becomes $V_{O(\min)}$ if $v_S > 0$ and $V_{O(\max)}$ if $v_S < 0$. The circuit shown in Fig. 6.53(a) compares the input signal v_S with the reference signal $V_{\text{ref}} = 0$, and if the input signal is greater than or less than zero, the output changes its value. This circuit is known as a *hard limiter*.

FIGURE 6.53 Hard limiter

The equations given earlier for adjustable voltage limiters can be applied to the limiter in Fig. 6.53(a), except that $R_F = \infty$ and the gain $A_f = -R_F/R_1$ is very large, tending to infinity. The transfer characteristic is shown in Fig. 6.53(b). The voltage limiting can also be accomplished by connecting two zener diodes, as shown in Fig. 6.54(a), for which $V_{O(\text{max})} = (V_{Z1} + V_D)$ and $V_{O(\text{min})} = -(V_{Z2} + V_D)$. Practical circuits exhibit finite slopes beyond the breaks because of the finite resistances of the zener diodes. These finite slopes are represented in Fig. 6.54(b) by light lines.

FIGURE 6.54
Zener hard limiter**EXAMPLE 6.18****D****Designing a hard voltage limiter**

(a) Design a hard limiter like the one in Fig. 6.53(a). The circuit should limit the negative output voltage to $V_{O(\text{min})} = -5\text{ V}$ and the positive output voltage to $V_{O(\text{max})} = 5\text{ V}$. The magnitude of the slopes after the break points should be less than or equal to $1/20$. The diode drop is $V_D = 0.7\text{ V}$. The dc supplies are given by $V_A = V_B = 12\text{ V}$. Determine the values of R_1 , R_2 , R_3 , R_4 , and R_5 .

(b) Use PSpice/SPICE to plot the transfer characteristic. Assume $V_{CC} = 12\text{ V}$, $-V_{EE} = -12\text{ V}$, and $v_s = -6\text{ to }6\text{ V}$.

SOLUTION

(a) Choose $R_1 = 10\text{ k}\Omega$. Since the slope $S_1 = R_3/R_1 = 1/20$,

$$R_3 = R_1/20 = 10\text{ k}\Omega/20 = 500\text{ }\Omega$$

From Eq. (6.92),

$$-5 = -0.7 - (12 + 0.7)R_3/R_2$$

$$R_3/R_2 = 0.3386$$

$$R_2 = 1477 \Omega$$

Since the slope $S_2 = R_5/R_1 = 1/20$,

$$R_5 = R_1/20 = 10 \text{ k}\Omega/20 = 500 \Omega$$

From Eq. (6.97),

$$5 = 0.7 + (12 + 0.7)R_5/R_4$$

$$R_5/R_4 = 0.3386$$

$$R_4 = 1477 \Omega$$

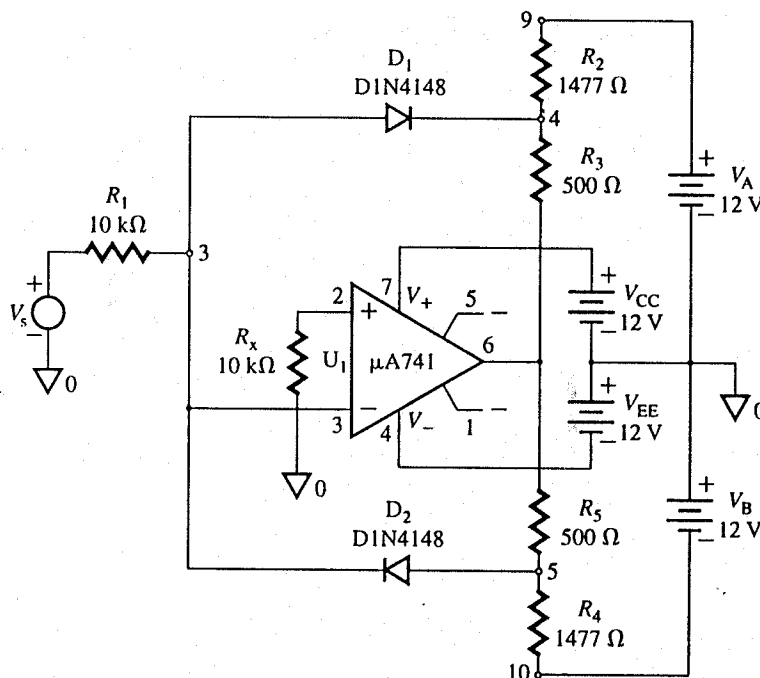
(b) The hard limiter for PSpice simulation is shown in Fig. 6.55. The list of the circuit file is as follows.

Example 6.18 Voltage Hard Limiter

```

VI 1 0 DC 6V
VCC 7 0 DC 12V
VEE 0 8 DC 12V
VA 9 0 DC 12V
VB 0 10 DC 12V
R1 1 3 12.5K
R2 4 9 1477
R3 4 6 500
R5 5 6 500
R4 5 10 1477
RX 2 0 10K
D1 3 4 DMOD ; Diode with model DMOD
D2 5 3 DMOD
.MODEL DMOD D ; Diode model with default parameters
.LIB NOM.LIB ; Referring to PSpice library file NOM.LIB for
               ; UA741 op-amp model
  
```

FIGURE 6.55 Comparator circuit for PSpice simulation



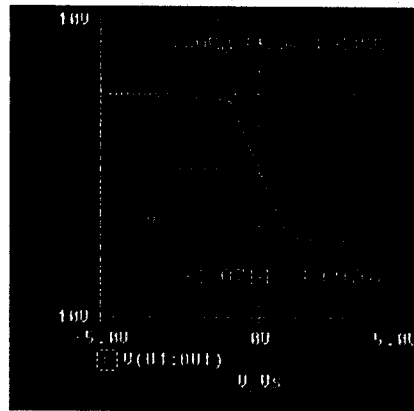

```

XA1 2 3 7 8 6 UA741      ; Subcircuit call for op-amp UA741
* vi+ vi- +vcc -vee vo
.DC VI -6V 6V 0.05V      ; dc sweep from -6 V to 6 V
.PROBE                    ; Graphics post-processor
.END

```

The transfer characteristic is shown in Fig. 6.56, which gives $V_{S(\max)} = 1.07$ V, $V_{S(\min)} = -0.96$ V, $V_{O(\max)} = 4.54$ V, and $V_{O(\min)} = -4.61$ V. Discrepancies between the design values and the PSpice results come from use of an ideal op-amp versus a macromodel and use of a specific diode versus a diode of type D1N4148. If we used ideal diodes, the transfer characteristic would be sharper.

FIGURE 6.56 PSpice transfer characteristic for Example 6.18



KEY POINTS OF SECTION 6.6

- A diode has a voltage drop, typically 0.7 V, which affects the waveforms of voltage and currents in a circuit. However, when a diode is placed inside the feedback path of an op-amp circuit, the effective voltage drop becomes negligible, on the order of μ V. The diode is then called a superdiode. Superdiodes are generally used for precision signal processing.
- The output voltage of an op-amp circuit can be clamped to a certain level by connecting a diode in parallel with the feedback resistance R_F . If we make $R_F = \infty$, the voltage gain $A_f = \infty$ and the output voltage swings from V_{sat} to $-V_{\text{sat}}$ as the input voltage v_i crosses zero.

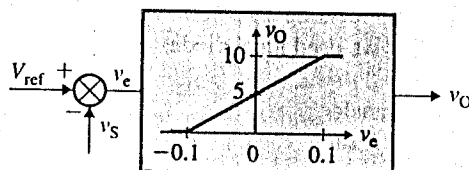
6.7 ► Op-Amp Circuit Design

So far, we have designed numerous op-amp circuits. Once the circuit configuration was known, the task was to find the component values. Since the output is dependent mostly on external components, one often has to choose some components before a final solution can be found. Generally, in a practical design problem, the circuit diagrams are not known. A designer must decide on the type of configuration, and alternative solutions are possible. In addition, like any other design problem, designing an op-amp circuit requires weighing alternative solutions and comparing complexity and costs. The design sequence can be summarized as follows:

- Step 1.** Study the problem.
- Step 2.** Create a block diagram of the solution.
- Step 3.** Find a hand-analysis circuit-level solution.
- Step 4.** Use PSpice/SPICE for verification.
- Step 5.** Construct the circuit in the lab and take measurements.

EXAMPLE 6.19**D**

Designing a proportional controller A control system requires a proportional controller that will produce $v_O = 5$ V if the error signal $v_e = 0$, $v_O = 0$ if $v_e \leq -0.1$ V, and $v_O = 10$ V if $v_e \geq 0.1$ V. These requirements are graphed in Fig. 6.57. Design a circuit that will implement this control strategy.

FIGURE 6.57 Proportional controller

$$\text{Problem: } v_O = 50V_{\text{ref}} - 50v_s + 5$$

SOLUTION

Step 1. Study the problem. The output voltage is related to the error voltage by

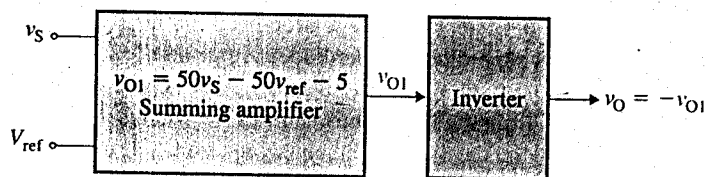
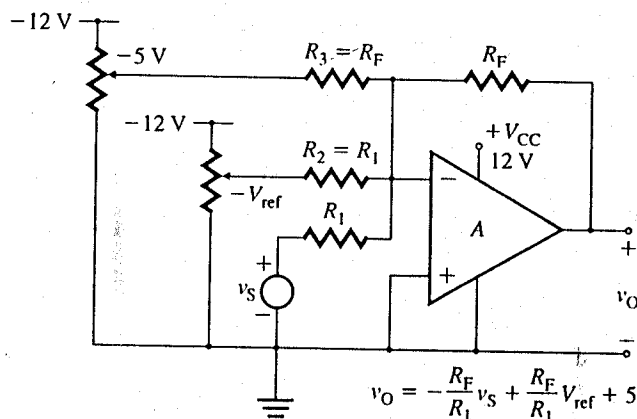
$$v_O = 50v_e + 5 = 50(V_{\text{ref}} - v_s) + 5 = 50V_{\text{ref}} - 50v_s + 5$$

Step 2. Create a block diagram of the solution. The problem requires a summing amplifier, as shown in Fig. 6.58(a). Since the signal v_s is expected to be positive, we also need an inverter.

Step 3. Devise a hand-analysis circuit-level solution. The inverting summing amplifier and the circuit implementation are shown in Fig. 6.58(b). Let $R_1 = R_2 = 10$ k Ω , $R_F = 50R_1 = 500$ k Ω , and $R_3 = R_F = 500$ k Ω . Choose $V_{CC} = 12$ V. Since the maximum output voltage is 10 V, there is no need for a voltage-limiting circuit.

Step 4. Use PSpice/SPICE for verification. You are encouraged to plot v_O against v_s for $v_s = 4.8$ V to 5.2 V in increments of 0.05. Invoke dc sweep with the following statement:

```
.DC VS 4.8 5.2 0.05
```

FIGURE 6.58 Solution to Example 6.19**(a) Block diagram****(b) Circuit implementation**

Summary

An op-amp is a high-gain differential amplifier that can be used to perform various functions in electronic circuits. Op-amps are normally used with a feedback circuit, and the output voltage becomes almost independent of the op-amp parameters. The basic configurations of op-amp amplifiers can be used in many applications such as integrators, differentiators, inductance simulators, meters, limiters, detectors, comparators, and precision rectifiers.

The analysis of an op-amp circuit can be simplified by assuming ideal characteristics. An ideal op-amp has a very high voltage gain, a very high input resistance, a very low output resistance, and a negligible input current. The characteristics of practical op-amps differ from the ideal characteristics, but analyses based on the ideal conditions are valid for many applications and provide the starting point for practical circuit design. Although the dc model of op-amps can be used to analyze complex op-amp circuits, it does not take into account the frequency dependency and op-amp nonlinearities. If the op-amp is operated at frequencies higher than the op-amp break frequency, the effect of frequency dependency should be evaluated.

The op-amp macromodel gives better accuracy. However, the student version of PSpice allows simulation of an amplifier with only one op-amp. If the limit is reached, then use of the ac model is recommended. The dc model should be the last choice unless the input signal is dc.

References

1. J. R. Hufault, *Op-Amp Network Design*. New York: John Wiley & Sons Inc., 1986.
2. F. W. Hughes, *Op-Amp Handbook*. Englewood Cliffs, NJ: Prentice Hall Inc., 1986.
3. C. F. Wojslow, *Operational Amplifiers*. New York: John Wiley & Sons Inc., 1986.
4. W. P. Vrbancis, "The operational amplifier summer—a practical design procedure." *WESCON Conference Record* (Session 2, 1982): 1–4.
5. *Linear Circuits—Operational Amplifier Macromodels*. Dallas: Texas Instruments, 1990.
6. G. Boyle, B. Cohn, D. Pederson, and J. Solomon, "Macromodeling of integrated circuit operational amplifiers." *IEEE Journal of Solid-State Circuits*, Vol. SC-9, No. 6 (December 1974): 353–64.
7. S. Progozy, "Novel applications of SPICE in engineering education." *IEEE Trans. on Education*, Vol. 32, No. 1 (February 1990): 35–38.

Review Questions

1. What are the characteristics of an ideal op-amp?
2. What is the minimum number of terminals in an op-amp?
3. What is the typical open-loop voltage gain of an op-amp?
4. What is the typical input resistance of an op-amp?
5. What are the saturation voltages of an op-amp?
6. What is the purpose of supply voltages in an op-amp?
7. What is the PSS of an op-amp?
8. What is the CMRR of an op-amp?
9. What is the difference between a closed-loop gain and an open-loop gain?
10. What is the virtual ground of an op-amp?
11. What is the integration time constant?
12. What is the frequency response of an integrator?
13. What is the differentiator gain constant?
14. What are the problems of a differentiator?
15. What is the frequency response of a differentiator?
16. What is a voltage follower?
17. What are the advantages of a voltage follower?
18. What is the significance of negative resistance?
19. What is a weighted summing amplifier?
20. What is a voltage limiter?
21. What is a soft limiter?
22. What is a clamper?

23. What is a comparator?
24. What is a limiting comparator?
25. What are the advantages of precision rectifiers?
26. What is a superdiode?

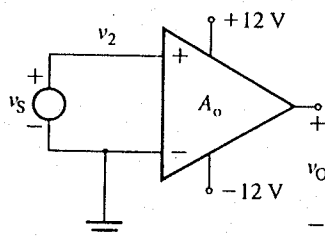
Problems

The symbol **D** indicates that a problem is a design problem. The symbol **P** indicates that you can check the solution to a problem using PSpice/SPICE or Electronics Workbench.

► 6.2 Characteristics of Ideal Op-Amps

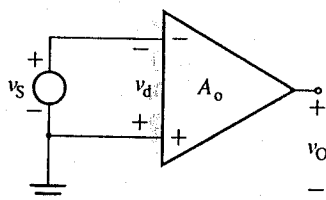
- 6.1 The op-amp in Fig. 6.1(a) has an open-loop gain of $A_o = 2 \times 10^5$. The input resistance is $R_i = 2 \text{ M}\Omega$. The dc supply voltages are $V_{CC} = 15 \text{ V}$ and $-V_{EE} = -15 \text{ V}$.
 - (a) What value of v_d will saturate the amplifier?
 - (b) What is the value of op-amp input currents i_i ?
- 6.2 The op-amp shown in Fig. P6.2 is used as a noninverting amplifier. The values are $A_o = 10^5$, $V_{CC} = 12 \text{ V}$, and $-V_{EE} = -12 \text{ V}$. If $v_s = 50 \mu\text{V}$, determine the output voltage v_o .

FIGURE P6.2



- 6.3 The op-amp shown in Fig. P6.3 is used as an inverting amplifier. The values are $A_o = 10^5$, $V_{CC} = 12 \text{ V}$, and $-V_{EE} = -12 \text{ V}$. If $v_s = 10 \mu\text{V}$, determine the output voltage v_o .

FIGURE P6.3



- 6.4 The op-amp in Fig. 6.3(a) has the following specifications: $A_o = 2 \times 10^5$, $R_i = 2 \text{ M}\Omega$, $R_o = 75 \Omega$, $V_{CC} = 15 \text{ V}$, $-V_{EE} = -15 \text{ V}$, and maximum output voltage swing $= \pm 14 \text{ V}$. If $v_+ = 0 \text{ V}$ and $v_- = 2 \sin 377t$, plot the instantaneous output voltage v_o .
- 6.5 The op-amp in Fig. 6.3(a) has the following specifications: $A_o = 2 \times 10^5$, $R_i = 2 \text{ M}\Omega$, $R_o = 75 \Omega$, $V_{CC} = 15 \text{ V}$, $-V_{EE} = -15 \text{ V}$, and maximum output voltage swing $= \pm 14 \text{ V}$. If $v_+ = 75 \mu\text{V}$ and $v_- = -25 \mu\text{V}$, determine the output voltage v_o .

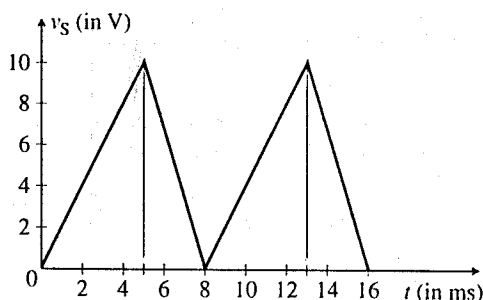
► 6.3 Op-Amp PSpice/SPICE Models

- P** 6.6 Develop PSpice/SPICE subcircuits for the dc model (in Fig. 6.5) and the ac model (in Fig. 6.6) for the LF411 op-amp. The parameters are $R_i = 10^{12} \Omega$, $R_o = 50 \Omega$, $A_o = 2 \times 10^5$, break frequency $f_b = 20 \text{ Hz}$, and unity-gain bandwidth $f_{bw} = 4 \text{ MHz}$. Assume dc power supply voltages of $\pm 15 \text{ V}$.
- P** 6.7 Develop PSpice/SPICE subcircuits for the dc model (in Fig. 6.5) and the ac model (in Fig. 6.6) for the LM324 op-amp. The parameters are $R_i = 2 \text{ M}\Omega$, $R_o = 50 \Omega$, $A_o = 2 \times 10^5$, break frequency $f_b = 4 \text{ kHz}$, and unity-gain bandwidth $f_{bw} = 1 \text{ MHz}$. Assume a dc supply voltage of $+15 \text{ V}$.

► 6.4 Analysis of Ideal Op-Amp Circuits

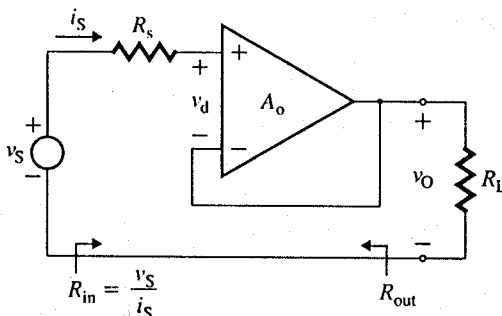
- D** 6.8 Design a noninverting amplifier as shown in Fig. 6.7(a) to provide a closed-loop voltage gain of $A_f = 100$. The input voltage is $v_s = 100$ mV with a source resistance of $R_s = 1$ k Ω . Find the value of output voltage v_o . The dc supply voltages are given by $V_{CC} = V_{EE} = 15$ V. Assume an ideal op-amp.
- P** 6.9 With the design values in Prob. 6.8, find the output voltage v_o , the input resistance $R_{in} = v_s/i_s$, and the output resistance R_{out} under the following conditions:
- $A_o = 25 \times 10^3$, $R_i = 10^{12}$ Ω , and $R_o = 50$ Ω
 - $A_o = 5 \times 10^5$, $R_i = 10^{12}$ Ω , and $R_o = 50$ Ω
 - Use PSpice/SPICE to verify your results in parts (a) and (b).
- 6.10 Design a noninverting amplifier as shown in Fig. 6.7(a) by determining the values of R_F and R_1 . The closed-loop gain should be $A_f = 10$. The input voltage to the amplifier is $v_s = 500$ mV, and it has a source resistance of 200 Ω . What is the value of output voltage v_o ?
- 6.11 The input voltage to the noninverting amplifier in Fig. 6.7(a) is shown in Fig. P6.11. The source resistance R_s is negligible, $R_F = 20$ k Ω , $R_1 = 5$ k Ω , $V_{CC} = 15$ V, and $-V_{EE} = -15$ V. Plot the output voltage v_o if $R_F = 20$ k Ω and $R_1 = 5$ k Ω .

FIGURE P6.11



- 6.12 The noninverting op-amp amplifier in Fig. 6.7(a) has an open-loop gain of $A_o = 5 \times 10^3$, $R_i = 10$ k Ω , and $R_F = 30$ k Ω . Calculate (a) the closed-loop voltage gain A_f , (b) the output voltage v_o , and (c) the error in output voltage if A_o is assumed to be infinite.
- 6.13 The input voltage to the noninverting amplifier in Fig. 6.7(a) is $v_s = 10 \sin(2000\pi t)$. The source resistance R_s is negligible. If $R_F = 20$ k Ω , $R_1 = 5$ k Ω , $V_{CC} = 15$ V, and $-V_{EE} = -15$ V, plot the output voltage v_o .
- 6.14 A voltage follower is shown in Fig. P6.14. The op-amp parameters are $A_o = 5 \times 10^5$, $R_o = 75$ Ω , and $R_i = 2$ M Ω . The input voltage v_s is $v_s = 5$ V, and $R_s = 10$ k Ω . Find the output voltage v_o , the input resistance $R_{in} = v_s/i_s$, and the output resistance R_{out} .

FIGURE P6.14



- D** 6.15 A transducer produces a voltage signal of $v_s = 50$ mV and has an internal resistance of $R_s = 5$ k Ω . Design the inverting op-amp amplifier of Fig. 6.9 by determining the values of R_1 , R_F , and R_X . The output voltage should be $v_o = -5$ V. The current drawn from the transducer should not be more than 20 μ A. Assume an ideal op-amp and $V_{CC} = V_{EE} = 12$ V.

- P** 6.16 With the design values in Prob. 6.15, find the value of output voltage v_O , the input resistance $R_{in} = v_S/i_S$, and the output resistance R_{out} under the following conditions:
- $A_o = 25 \times 10^3$, $R_i = 10^{12} \Omega$, and $R_o = 50 \Omega$
 - $A_o = 5 \times 10^5$, $R_i = 10^{12} \Omega$, and $R_o = 50 \Omega$
 - Use PSpice/SPICE to verify your results in parts (a) and (b).
- 6.17 The inverting amplifier in Fig. 6.9 has $R_1 = 5 \text{ k}\Omega$, $R_F = \infty$, $R_x = 5 \text{ k}\Omega$, $V_{CC} = 15 \text{ V}$, $-V_{EE} = -15 \text{ V}$, and maximum output voltage swing $= \pm 14 \text{ V}$. If $v_S = 200 \text{ mV}$, determine the output voltage v_O .
- 6.18 The inverting amplifier in Fig. 6.9 has $R_1 = 10 \text{ k}\Omega$, $R_F = 50 \text{ k}\Omega$, and $R_x = 8.33 \text{ k}\Omega$. The op-amp has an open-loop voltage gain of $A_o = 2 \times 10^5$. The input voltage is $v_S = 100 \text{ mV}$. Calculate (a) the closed-loop gain A_F , (b) the output voltage v_O , and (c) the error in output voltage if the open-loop gain A_o is assumed infinite.
- D** 6.19 Two transducers produce voltage signals of $v_b = 200 \text{ mV}$ and $v_a = 220 \text{ mV}$. Design a differential amplifier as shown in Fig. 6.10 to produce an output voltage $|v_O| = 5 \text{ V}$. Assume an ideal op-amp and $V_{CC} = V_{EE} = 12 \text{ V}$.
- P** 6.20 With the design values in Prob. 6.19, find the value of output voltage v_O under the following conditions of the op-amp:
- $A_o = 25 \times 10^3$ and $R_i = 10^{12} \Omega$
 - $A_o = 5 \times 10^5$ and $R_i = 10^{12} \Omega$
 - Use PSpice/SPICE to verify your results in parts (a) and (b).
- D** 6.21 (a) Design a differential amplifier as shown in Fig. 6.10 to give a differential voltage gain of $|A_F| = 200$. The input voltage are $v_b = 70 \text{ mV}$ and $v_a = 50 \text{ mV}$. Assume an ideal op-amp and $V_{CC} = V_{EE} = 12 \text{ V}$.
- (b) Calculate the error in output voltage if the open-loop gain is $A_o = 5 \times 10^5$.
- 6.22 The values of the differential amplifier in Fig. 6.10 are $A_o = 5 \times 10^5$, $R_1 = 5 \text{ k}\Omega$, $R_F = 50 \text{ k}\Omega$, $R_a = 2 \text{ k}\Omega$, and $R_x = 20 \text{ k}\Omega$. The input voltages are $v_b = 5 \text{ mV}$ and $v_a = -15 \text{ mV}$. Find the output voltage v_O .

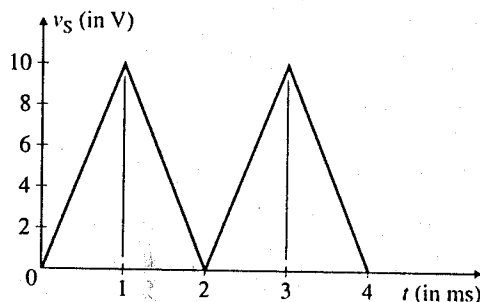
► **6.5 Op-Amp Applications**

- 6.23 The integrator in Fig. 6.13 has $V_{CC} = 15 \text{ V}$, $-V_{EE} = -15 \text{ V}$, maximum voltage swing $= \pm 14 \text{ V}$, $C_F = 0.01 \mu\text{F}$, $R_1 = 1 \text{ k}\Omega$, and $R_F = 1 \text{ M}\Omega$. The initial capacitor voltage is $V_{co} = 0 \text{ V}$. Draw the waveform for the output voltage if the input voltage is described by

$$v_S = \begin{cases} 1 \text{ V} & \text{for } 0 \leq t < 1 \text{ ms} \\ -1 \text{ V} & \text{for } 1 \leq t < 2 \text{ ms} \\ 1 \text{ V} & \text{for } 2 \leq t < 3 \text{ ms} \\ -1 \text{ V} & \text{for } 3 \leq t < 4 \text{ ms} \end{cases}$$

- 6.24 The integrator in Fig. 6.13 has $V_{CC} = 15 \text{ V}$, $-V_{EE} = -15 \text{ V}$, maximum voltage swing $= \pm 14 \text{ V}$, $C_F = 0.1 \mu\text{F}$, $R_1 = 10 \text{ k}\Omega$, and $R_F = 1 \text{ M}\Omega$. The initial capacitor voltage is $V_{co} = 0 \text{ V}$. Draw the waveform of the output voltage for the input voltage shown in Fig. P6.24.

FIGURE P6.24



- 6.25 The integrator in Fig. 6.13 has $C_F = 0.01 \mu\text{F}$, $R_1 = 10 \text{ k}\Omega$, and $R_F = 1 \text{ M}\Omega$. The open-loop voltage gain of the op-amp is $A_o = 5 \times 10^5$. Use Miller's theorem to find the 3-dB frequency of the integrator.

- D** 6.26 Design an integrator as shown in Fig. 6.13 to be operated with an ac signal of 5 kHz and to give a voltage gain of 10 at $\omega = 1$ rad/s.
- D** 6.27 (a) Design a differentiator as shown in Fig. 6.21(a) to satisfy the following specifications: maximum voltage gain of $A_{f(\max)} = 20$ and gain limiting frequency $f_b = 10$ kHz. Determine the values of R_1 , R_F , and C_1 .
(b) Use PSpice/SPICE to check your results by plotting the frequency response in part (a).
- 6.28 The differentiator in Fig. 6.21(a) has $R_1 = 2$ k Ω , $R_F = 10$ k Ω , and $C_1 = 0.01$ μ F. Determine (a) the differentiator time constant τ_d , (b) the gain limiting frequency f_b , and (c) the maximum closed-loop voltage gain $A_{f(\max)}$.
- D** 6.29 Design an instrumentation amplifier as shown in Fig. 6.24 to give a differential voltage gain A_f between 500 and 1000.
- D** 6.30 Design an instrumentation amplifier as shown in Fig. 6.25 to give a fixed differential voltage gain of $A_f = 750$.
- 6.31 The noninverting summing amplifier in Fig. 6.26 has $R_a = R_b = R_c = 20$ k Ω , $R_F = 40$ k Ω , $R_B = 20$ k Ω , $v_a = 2$ V, $v_b = -3$ V, $v_c = -2$ V, $V_{CC} = 15$ V, $-V_{EE} = -15$ V, and maximum voltage swing = ± 14 V. Determine the output voltage v_O .
- 6.32 The inverting summing amplifier in Fig. 6.27 has $R_1 = R_2 = R_3 = 20$ k Ω , $R_F = 40$ k Ω , $R_x = 5.71$ k Ω , $v_1 = 2$ V, $v_2 = -3$ V, $v_3 = -2$ V, $V_{CC} = 15$ V, $-V_{EE} = -15$ V, and maximum voltage swing = ± 14 V. Determine the output voltage v_O .
- D** 6.33 Design an add-subtract summing amplifier as shown in Fig. 6.28 to give an output voltage of the form $v_O = 5v_a + 7v_b + 3v_c - 2v_1 - v_2 - 6v_3$. The equivalent resistance R_A should be set to 20 k Ω .
- D** 6.34 Design an add-subtract summing amplifier as shown in Fig. 6.28 to give an output voltage of the form $v_O = 5v_a + 9v_b + 3v_c - 8v_1 - 2v_2 - 6v_3$. The minimum value of any resistance should be $R_{\min} = 20$ k Ω .
- D** 6.35 Design an optocoupler drive circuit as shown in Fig. 6.29 to produce a drive current of 500 mA from a signal voltage of 10 mV.
- D** 6.36 Design a photodetector circuit as shown in Fig. 6.30 to give an output voltage of 1 V at an incident power density of $D_p = 1$ μ W/cm². The current responsivity of the photodiode is $D_i = 1$ A/W, and the active area is $a = 40$ mm².
- 6.37 The voltage-to-current converter in Fig. 6.31 has $R_1 = R = 10$ k Ω and $v_S = 200$ mV. Determine the load current i_L .
- 6.38 The full-scale current of the moving coil for the dc voltmeter in Fig. 6.32 is $I_M = 200$ μ A. Determine the value of R_1 to give a full-scale reading of $V_S = 300$ V.
- D** 6.39 Design a dc millivoltmeter as shown in Fig. 6.33. The full-scale current of the moving coil is $I_M = 0.5$ μ A. Determine the values of R_1 , R_F , and R_2 to give a full-scale voltage reading of $V_S = 200$ V.
- D** 6.40 Design a negative impedance converter as shown in Fig. 6.34 by determining the component values such that the input resistance will be $Z_{in} = R_{in} = -15$ k Ω .
- D** 6.41 (a) The noninverting integrator in Fig. 6.36(a) has $V_{CC} = 15$ V, $-V_{EE} = -15$ V, maximum voltage swing = ± 14 V, $C = 0.01$ μ F, and $R_1 = R_F = R = 1$ M Ω . The initial capacitor voltage is $V_{co} = 0$ V. Draw the waveform for the output voltage if the input is a step voltage described by $v_S = 1$ V for $t \geq 0$.
(b) Use PSpice/SPICE to plot the output voltage in part (a).
- D** 6.42 Design an inductance simulator as shown in Fig. 6.37 by determining the values of components. The inductance should be $L_e = 2$ mH.
- **6.6 Circuits with Op-Amps and Diodes**
- P** 6.43 (a) The precision full-wave rectifier in Fig. 6.44(a) has $R_1 = R_2 = R_F = R = 10$ k Ω , $R_3 = 40$ k Ω , and $R_4 = 40$ k Ω . The input voltage is $v_S = 2 \sin 377t$. Plot the transfer characteristic, and draw the waveform of the output voltage v_O .
(b) Use PSpice/SPICE to plot the transfer characteristic and the output voltage.
- D** 6.44 (a) Design a precision full-wave rectifier as shown in Fig. 6.44(a) to provide a voltage gain of $A_f = v_O/v_S = 50$. The input voltage is $v_S = 0.01 \sin(200\pi t)$.
(b) Use PSpice/SPICE to check your design by plotting the output voltage.

D P 6.45

- (a) Design a negative voltage limiter using the circuit in Fig. 6.48(a) by determining the values of R_1 , R_2 , R_3 , and R_F . The supply dc voltage is $V_A = 15$ V. The circuit should limit the negative output voltage to $V_{O(\min)} = -8$ V. The voltage gain without limiting is $A_f = -5$. The diode is fully turned on at a forward current of $i_D = 0.1$ mA, and its corresponding forward voltage drop is $V_D = 0.7$ V. The slope after the break point is to be limited to $S_1 = -1/30$.

- (b) Use PSpice/SPICE to plot the transfer characteristic for part (a).

6.46

The adjustable limiter in Fig. 6.49(a) has $R_1 = 12$ k Ω , $R_F = 70$ k Ω , $R_2 = 8$ k Ω , $R_3 = 1$ k Ω , $R_4 = 6$ k Ω , $R_5 = 1$ k Ω , $V_A = 15$ V, $-V_B = -15$ V, and $V_D = 0.7$ V. Determine (a) the positive clamping voltage $V_{O(\max)}$ and the corresponding input voltage $V_{S(\min)}$, (b) the negative clamping voltage $V_{O(\min)}$ and the corresponding input voltage $V_{S(\max)}$, and (c) the output voltage when the input voltage is $v_S = 5$ V.

D P 6.47

- (a) Design an adjustable voltage limiter as shown in Fig. 6.49(a) to satisfy the following specifications: $V_{O(\min)} = -5$ V, $V_{O(\max)} = 5$ V, voltage gain $A_f = -10$. The slope is $S_1 = -1/20$ after break for $v_S > 0$, and the slope is $S_2 = -1/20$ after break for $v_S < 0$. The dc supply voltages are $V_A = 12$ V and $-V_B = -12$ V. The on-state diode current is $i_D = 0.2$ mA, and the corresponding on-state diode voltage is $V_D = 0.7$.

- (b) Use PSpice/SPICE to plot the transfer characteristic. Assume $V_{CC} = 12$ V and $-V_{EE} = -12$ V. Use the PSpice/SPICE op-amp macromodel.

D P 6.48

Design an output voltage clamping circuit as shown in Fig. 6.52(a) so that the slope of the transfer characteristic is $S = v_O/v_S = 20$, $V_{O(\max)} = 6.7$ V, and $V_{O(\min)} = -8.7$ V. Determine the zener voltages V_{Z1} and V_{Z2} . Assume $V_D = 0.7$ V.

D P 6.49

- (a) Design a hard limiter as shown in Fig. 6.53(a) by determining the values of R_1 , R_2 , R_3 , R_4 , and R_5 . The circuit should limit the negative output voltage to $V_{O(\min)} = -6$ V and the positive voltage to $V_{O(\max)} = 6$ V. The magnitude of the slopes after the break points should be less than or equal to $1/25$. The diode drop is $V_D = 0.7$ V at $i_D = 0.1$ mA. The dc supplies are given by $V_A = -V_B = 15$ V.

- (b) Use PSpice/SPICE to plot the transfer characteristic. Assume $V_{CC} = 15$ V, $-V_{EE} = -15$ V, and $v_S = -5$ V to 5 V. Use the PSpice/SPICE op-amp macromodel.

D P 6.50

- (a) Design a hard limiter as shown in Fig. 6.53(a) by determining the values of R_1 , R_2 , R_3 , R_4 , and R_5 . The circuit should limit the negative output voltage to $V_{O(\min)} = -5$ V and the positive voltage to $V_{O(\max)} = 5$ V. The magnitude of the slopes after the break points should be less than or equal to $1/50$. The diode drop is $v_D = 0.7$ V at $i_D = 0.1$ mA. The dc supplies are given by $V_A = -V_B = 15$ V.

- (b) Use PSpice/SPICE to plot the transfer characteristic. Assume $V_{CC} = 15$ V, $-V_{EE} = -15$ V, and $v_S = -5$ V to 5 V. Use the PSpice/SPICE op-amp macromodel.

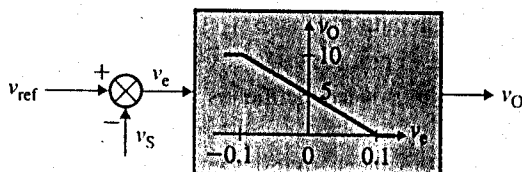
D P 6.51

- (a) Design a hard limiter as shown in Fig. 6.53(a) by determining the values of R_1 , R_2 , R_3 , R_4 , and R_5 . The circuit should limit the negative output voltage to $V_{O(\min)} = -7$ V and the positive voltage to $V_{O(\max)} = 9$ V. The magnitude of the slopes after the break points should be less than or equal to $1/50$. The diode drop is $v_D = 0.7$ V at $i_D = 0.1$ mA. The dc supplies are given by $V_A = -V_B = 15$ V.

- (b) Use PSpice/SPICE to plot the transfer characteristic. Assume $V_{CC} = 15$ V, $-V_{EE} = -15$ V, and $v_S = -5$ V to 5 V. Use the PSpice/SPICE op-amp macromodel.

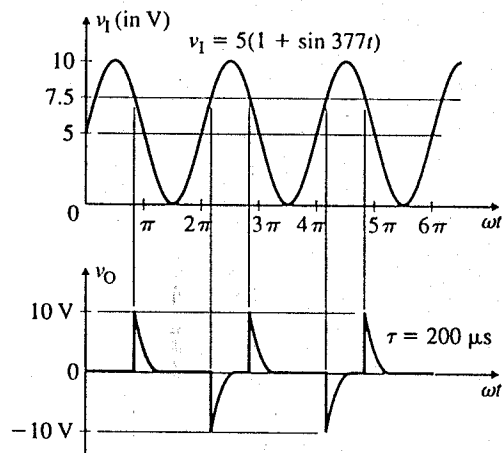
► **6.7 Op-Amp Circuit Design****D** 6.52

A control system requires a proportional controller that will produce $v_O = 5$ V if the error signal $v_e = 0$, $v_O = 10$ V if $v_e \leq -0.1$ V, and $v_O = 0$ V if $v_e = 0.1$ V. These requirements are graphed in Fig. P6.52. Design a circuit that will implement this control strategy to produce v_O from v_S and v_{ref} .

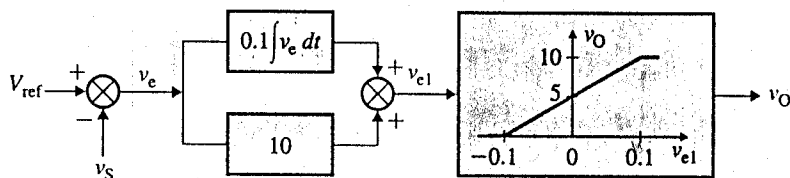
FIGURE P6.52

D 6.53

A triggering circuit requires short pulses v_O of approximately 10 V magnitude and pulse width of $t_w = 200 \mu\text{s}$, as shown in Fig. P6.53. Design a circuit that will generate triggering pulses. (There is no unique solution.)

FIGURE P6.53**D** 6.54

A control system requires a proportional and integral controller that will produce $v_O = 5 \text{ V}$ if the signal $v_{e1} = 0$, $v_O = 10 \text{ V}$ if $v_{e1} \leq -0.1 \text{ V}$, and $v_O = 0 \text{ V}$ if $v_{e1} \geq 0.1 \text{ V}$, as shown in Fig. P6.54. Design a circuit that will implement this control strategy to produce v_O from the reference signal v_S and the feedback signal v_{ref} .

FIGURE P6.54**D** 6.55

The inverting amplifier shown in Fig. P6.55 can give high voltage gain and requires a narrow range of resistor values. Output voltage should be $v_O = 12 \text{ V}$ for $v_S \leq -0.05 \text{ V}$ and $v_O = -12 \text{ V}$ if $v_S \geq 0.05 \text{ V}$. Design a circuit that will implement this control strategy.

FIGURE P6.55